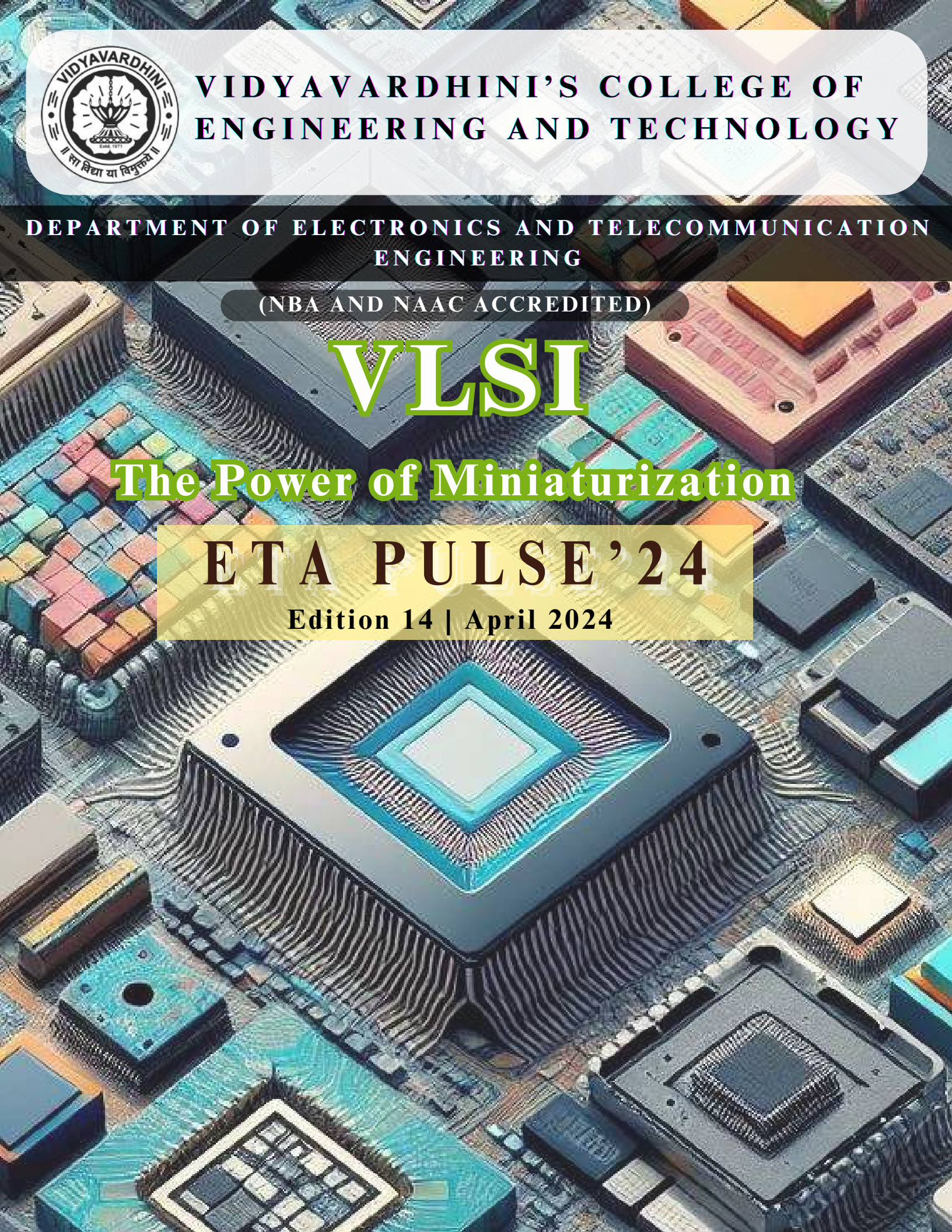

VIDYAVARDHINI'S COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION ENGINEERING

(NBA AND NAAC ACCREDITED)

VLSI

The Power of Miniaturization

ETA PULSE'24

Edition 14 | April 2024

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FROM THE HOD'S DESK

It gives me immense pleasure and honor to present the annual magazine of Electronics and Telecommunication Engineering department for the academic year 2023-24. It is the need of the hour that there should be focus and concentrated efforts towards the technical skills to be aligned with the fast-changing industrial scenario. The ETA Committee's efforts are exactly on this line and this year's ***PULSE Magazine****, the* ***14th edition,*** *is the fruitful result of their efforts.*
The department conducted training on advancements in technology in association with IIT Bombay, this has resulted in an increased number of students opting for assignments and jobs in core technical areas.

The PULSE is the reflection of dynamic changes in Industry and this year the theme is ***"VLSI- The Power of Miniaturization"****. This topic has gained exceptional developmental pace recently. Standing at the threshold of digitization and innovation, India's semiconductor industry is projected to achieve a market value of $55Bn by 2026. Semiconductor chip manufacturing is driven primarily by the demand for semiconductors in smartphones and wearables, automotive parts, and computers and data storage, which together make up over 60% of the market.*
The various activities and events planned and executed by the faculty members and students in association with ***IEEE VCET SB*** *and* ***IETE VCET SF*** *also contributed to the very essence of this mission. The Alumni Interviews, industry visits, technical activities in the form of events in the department along with industry interactions are the part of commendable content.*

Though it has been such a tough year due to the global crisis, we put forward our best efforts to shine bright with excellent exam results as well as placement in various reputed companies like Infosys, Capgemini, Zeus Learning, Feed Spot, Bristlecone, TCS, Zensar, Wipro, LTI, and many more. Building the magazine from the scratch by taking the clue from the predecessors and putting in efforts to excel and make the adorable ***PULSE*** *a reality is really the great teamwork by the* ***ETA Committee****.*
I appreciate the guiding work done by ***Mrs. Ashwini Katkar*** *the staff in charge of the ETA.*
My best regards to the entire ETA team and wish them success in their future activities.

Dr. Amrita Ruperee
HOD, EXTC

FROM STAFF INCHARGE'S DESK

Dear Readers,

Greetings from ETA Pulse! I am delighted to welcome you to our publication. At Pulse, we're passionate about exploring the latest advancements and breakthroughs in technology. We're also dedicated to showcasing the innovative work of our students and faculty, whether it's a cutting-edge startup or a groundbreaking research project, curricular or extracurricular achievements. Our goal is to inspire others to push boundaries and achieve greatness.

We know that college is a time of exploration, so our magazine is here to keep you updated on the latest trends and best practices in your field. Our articles are crafted to be informative and engaging, ensuring you stay informed while enjoying the ride.

The theme of ***Pulse'24*** *is* ***"VLSI- The Power of Miniaturization"****, encompassing a broad spectrum of topics ranging from introduction, to design, emerging technology, future trends, job opportunities, and more. In addition, we are pleased to feature interviews with our esteemed alumni who have achieved success in diverse fields.*

I would like to extend my sincere gratitude to ***Dr. Harish Vankudre****, our Principal, for his invaluable support, and to* ***Dr. Amrita Ruperee****, our HOD, EXTC, for her unwavering guidance and assistance. I would also like to commend the hard work of* ***Miss. Riddhi Garudkar****, our Secretary, and the entire team* ***'ETA'*** *for their dedicated efforts.*

I sincerely appreciate you to select our magazine as your go-to source for information and inspiration. Our dedication lies in delivering top-notch content and resources to meet your needs, and we eagerly anticipate receiving your valuable feedback and suggestions.

Happy Reading!

Mrs. Ashwini Sunil Katkar
Staff in Charge, ETA

FROM SECRETARY

Dear Readers,

"To give real service you must add something which cannot be bought or measured with money"

It is an inspiring quote from "Bharat Ratan Sir M. Visvesvaraya" which gives the essence of selflessness while giving the service, and I believe ETA is a committee that gives promising service to spread the light of knowledge to a wide extent by publishing its works. By following the legacy this year ETA is ready with great enthusiasm for publishing ***ETA PULSE '24*** *with the title* ***"VLSI- The Power of Miniaturization"****. This title is a part of core electronics and I hope the reader will get information and facts from this magazine. It covers a wide range of topics from* ***chronicles to trends****,* ***market analysis*** *to* ***future opportunities****, also articles from our alumni working in the domain, interviews of our very own alumni and many more.*

It was a gratifying moment for me to be a secretary of ETA and to lead the team. Last but foremost, I would like to express ***my gratitude to the HOD****, for her valuable support and* ***staff in charge for her endless encouragement****. Also, the unforgettable effort taken by every team member contributes a huge part to the completion of the magazine.*

Miss. Riddhi Garudkar
Secretary, ETA

INDEX

ESSENCE OF ELECTRONICS IN VLSI

Very-Large-Scale Integration (VLSI) is a revolutionary process that drastically transformed the electronics industry. It involves the creation of integrated circuits (ICs) by integrating thousands, and sometimes millions of microscopic transistors onto a single silicon semiconductor chip. Imagine a tiny city packed with electronic components! This allows us to build complex electronic systems like processors, memory, and even entire computers on a single chip.

VLSI design involves meticulously arranging these transistors and their connections to perform specific functions. It's the foundation for modern technology, powering everything from smartphones to supercomputers.

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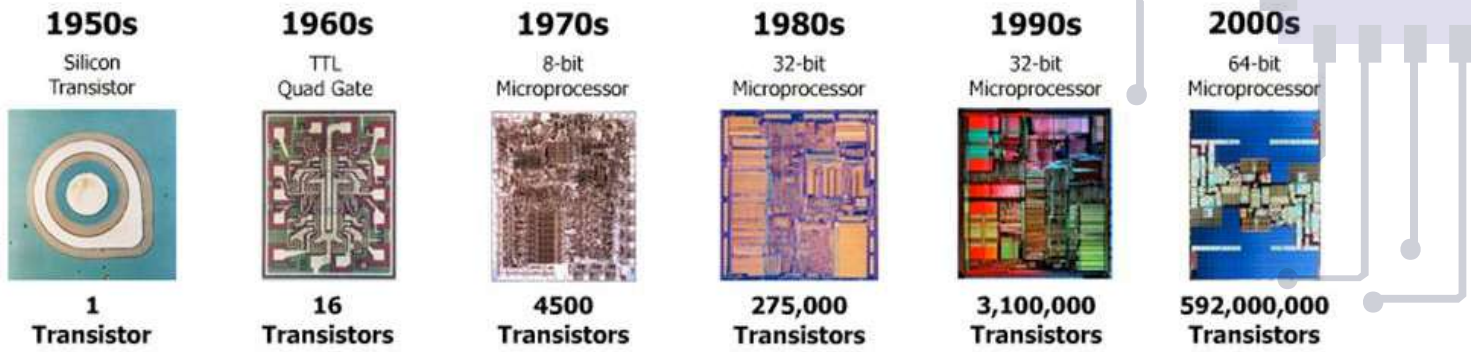
History of VLSI Design:



Evolution of computer processor design over time

Image Courtesy :-https://www.quora.com/How-have-advancements-in-semiconductor-technology-affected-the-design-of-computer-processors-over-time.

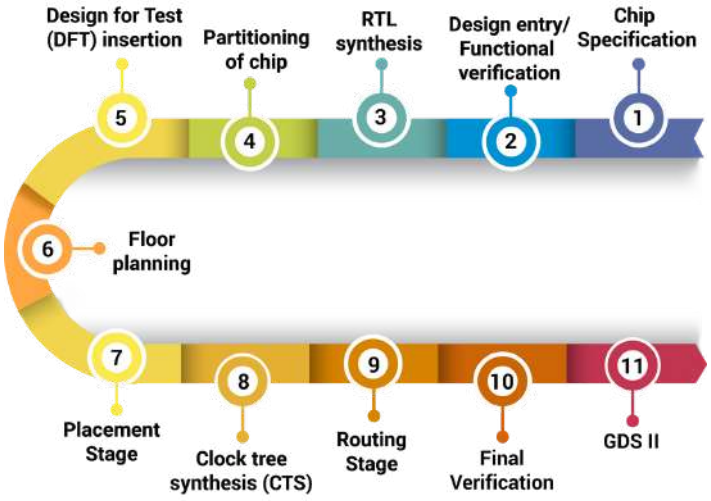
The history of VLSI design can be traced back to the 1950s when the first transistor was invented. Later on, in the 1960s, the first integrated circuit (IC) was developed which revolutionized the electronics industry. With the development of ICs, the size of electronic devices reduced drastically, and their functionality increased. In the 1970s, the first microprocessor was invented, which gave birth to the modern computer era. The 1980s saw the emergence of VLSI design as a discipline, and the first VLSI chip was designed in 1983. Since then, VLSI design has been advancing at a rapid pace, and the technology has evolved to produce more complex and efficient chips.

ASIC Design: The Backbone of Specialized Chips in VLSI

ASIC stands for Application Specific Integrated Circuits. In VLSI's world of millions of transistors, ASICs are custom-built chips that outperform general-purpose ones in speed, power, and size.

ASIC Design Flow:

1. **Define the Goal:** First, engineers outline the chip's functionalities and performance targets.
2. **Explore Approaches:** Different design options are considered to achieve the desired outcome.
3. **Code the Blueprint (RTL):** Hardware Description Language describes the chip's behavior using registers.
4. **Translate the Code:** This code is converted into a detailed circuit blueprint (netlist).
5. **Physical Layout:** The netlist is transformed into the chip's physical design, placing and connecting components efficiently.
6. **Double Check:** Rigorous simulations ensure the design functions as intended.
7. **Build and Test:** The final design is sent for fabrication and rigorously tested to identify and fix any errors.

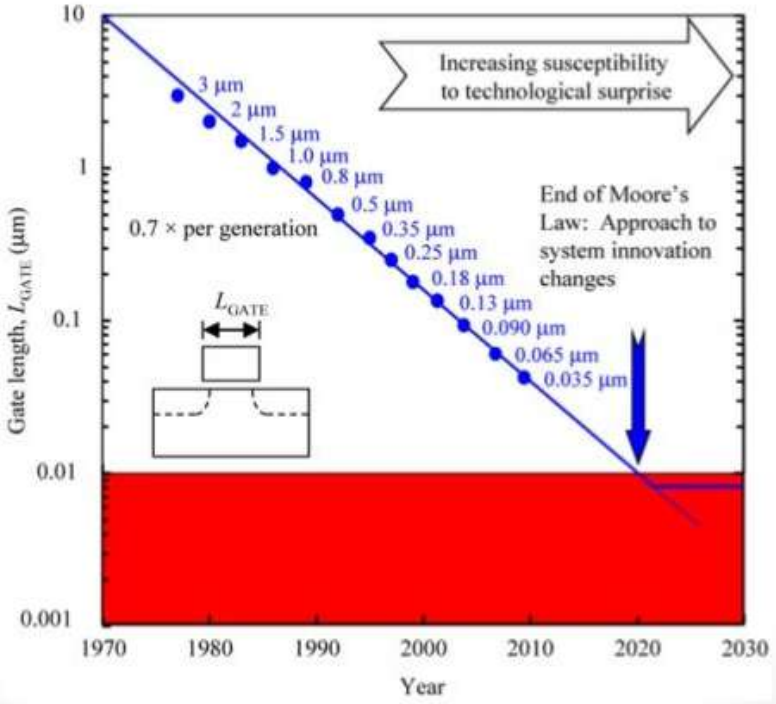


ASIC FLOW

Image Courtesy :- https://www.dwbtech.com/asic-flow.html

Theories proposed in VLSI

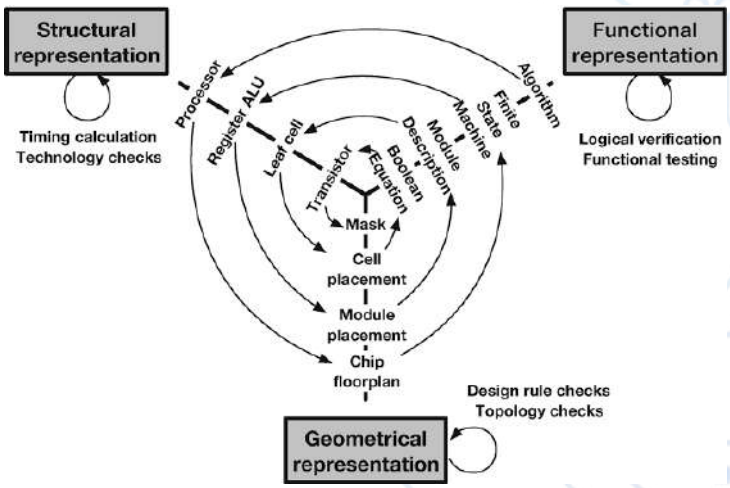
1) Moore's Law first observed by Gordon Moore, co-founder of Fairchild Semiconductor and Intel, in 1965.



End of Moore's Law

"The functionality of devices doubles every 18 months" or "the cost of the same functionality halves 18 months".

2) The Gajski-Kuhn Y-Chart model is a significant concept in the field of Electronic VLSI design. It was developed by Daniel Gajski and Robert Kuhn in 1983

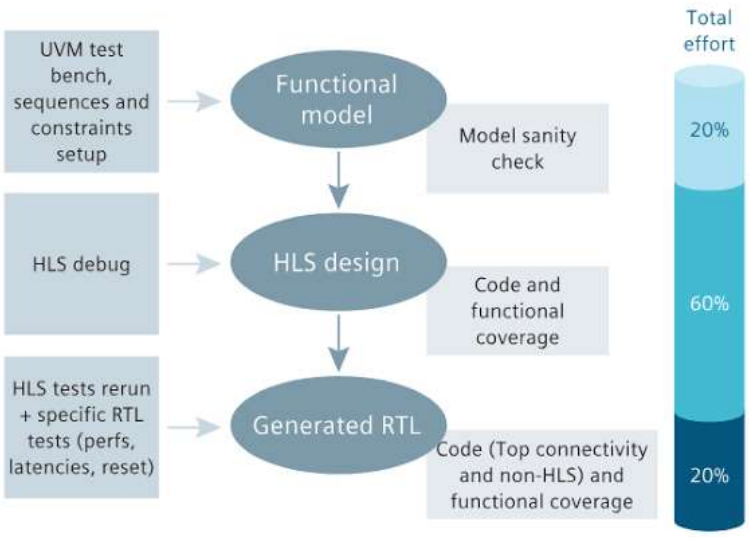


Gajski-Kuhn Y-chart

Image Courtesy :- https://www.tutorialspoint.com/vlsi_design/vlsi_design_digital_system.htm

HIGH-LEVEL SYNTHESIS

High-Level Synthesis (HLS) automates the creation of hardware from algorithms in VLSI. You describe the circuit's behavior in **C/C++/System C**, and the HLS tool generates a hardware architecture (RTL). This process speeds up the design compared to manual coding and allows you to explore different options without rewriting the code. The tool analyzes your code, identifies opportunities to run things concurrently, schedules operations, allocates hardware resources, and optimizes for performance, area, or power. Overall, HLS bridges the gap between algorithms and hardware, thereby improving design efficiency.

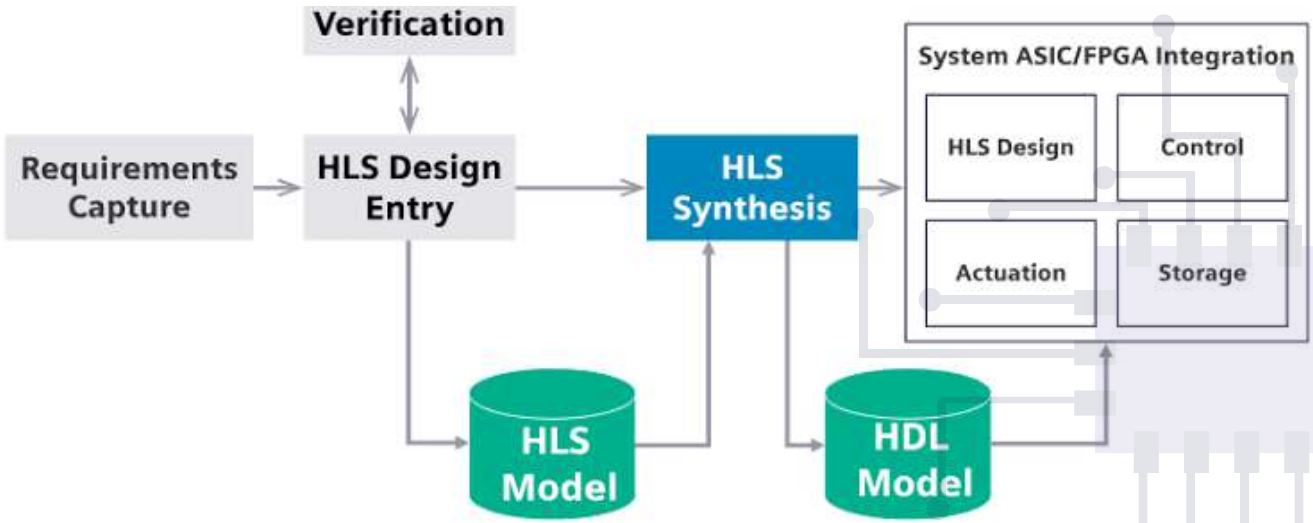


Automotive image signal processing to market with HLS

Image Courtesy :-https://resources.sw.siemens.com/en-US/white-paper-stmicroelectronics-brings-automotive-image-signal-processing-to-market-with-high-level-synthesis

Regularity,Modularity, Locality: Powerhouse Trio in VLSI Design

- **Regularity:** Like Legos, identical building blocks (logic gates) are used repeatedly for simpler design, fewer errors, and easier automation.
- **Modularity:** Complex circuits are broken into independent modules, each with a specific function and clear interfaces. This allows individual modules to be designed, tested, and reused efficiently, similar to building separate modules in a house.
- **Locality:** Frequently interacting modules are placed close together on the chip. This minimizes wire length, reducing signal delays and power consumption, just like placing the kitchen and dining room close together in a house reduces walking distance.
- **Testing and Verification:** With millions of transistors, exhaustive testing is impossible. Techniques like scan chains and BIST target potential problems, while verification uses math and simulations to ensure the design meets specifications.



Deploying HLS into a DO-254/ED-80 workflow

Image Courtesy:- https://eda.sw.siemens.com/en-US/ic/catapult-high-level-synthesis/resources/

LOW POWER DESIGN

The aim of low power VLSI design is to minimize the individual components of power as much as possible, hence decreasing the total power consumption of integrated circuits (ICs).

Key Areas of Focus in Low Power Design:

a) **Power Modeling**: Understanding and predicting power consumption patterns in VLSI circuits.

b)**Switching Activity**: Reducing the energy dissipated by charging and discharging internal node capacitances during transitions.

c)**Self-Transition and Coupling Transition**: Managing the transitions within and between circuits to minimize power loss.

d)**Dynamic Power Dissipation**: Addressing the power consumed during the operation of the circuit, particularly during state changes in logic circuits.

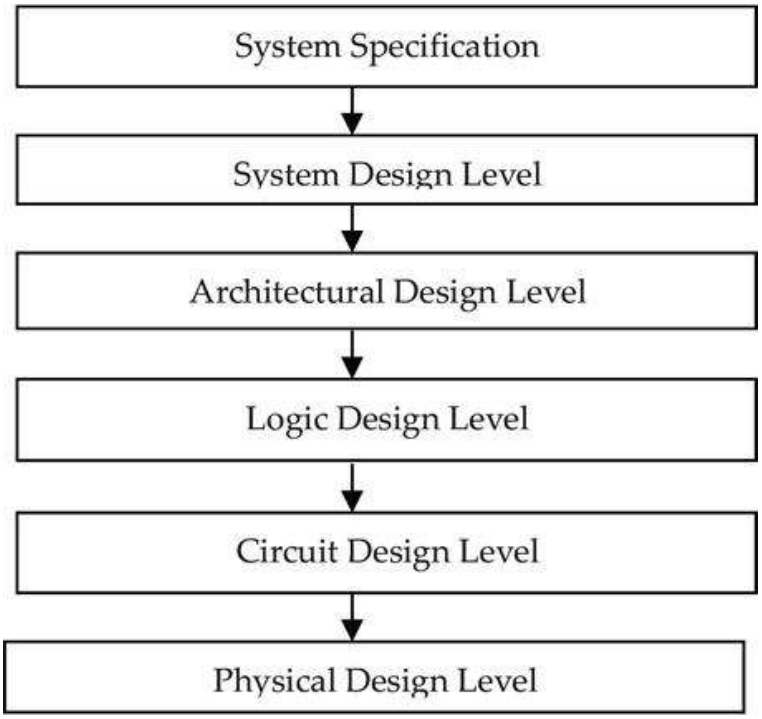
Design Methodologies:

Dynamic Voltage Scaling: Adjusting the voltage supplied to the circuit to reduce power consumption without compromising performance.

Power Gating: Temporarily turning off the power supply to parts of the circuit that are not in use.

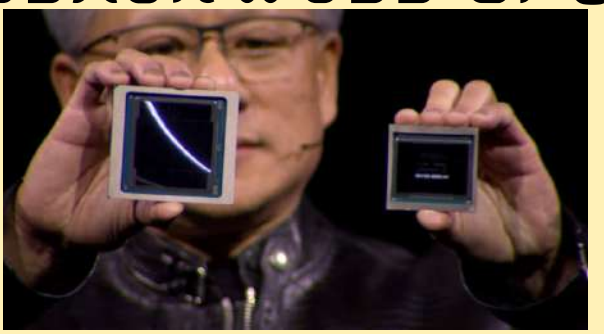
Clock Gating: Reducing the switching activity by disabling the clock signal in idle parts of the circuit.

Multi-Vdd and Multi-Vth Design: Using multiple threshold voltages and supply voltages to optimize power usage



Flow Chart of Low Power Design

NVIDIA'S BLACKWELL GPU

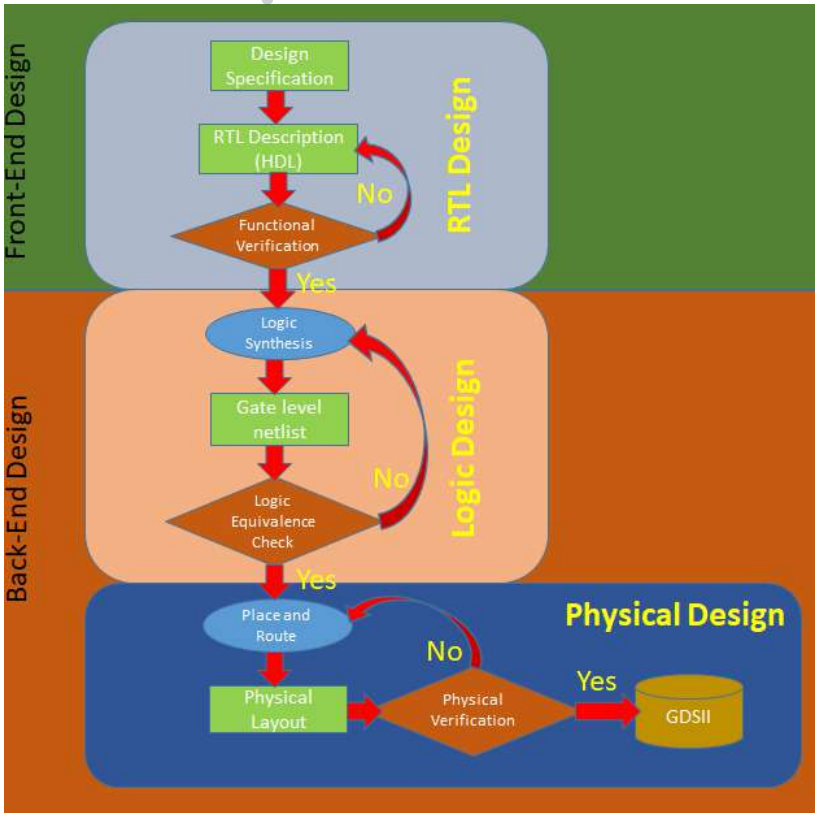


NVIDIA- Blackwell GPU Design

Did you know that in the latest NVIDIA's GTC keynote, NVIDIA released its Blackwell GPU which has 206 billion transistors, it is a new class of AI superchip, offering unprecedented performance, efficiency, and scale.

Image Courtesy :- https://justoborn.com/nvidia-blackwell/.

FRONT-END DESIGN AND BACK-END DESIGN



ASIC Design Flow

Image Courtesy :- https://www.linkedin.com/pulse/asic-backend-design-flow-vlsi-part-1-rtllogic-synthesis-priya-pandey.

VLSI design separates the creation process into two distinct stages: front-end and back-end design.

Front-End Design: The Architect's Domain

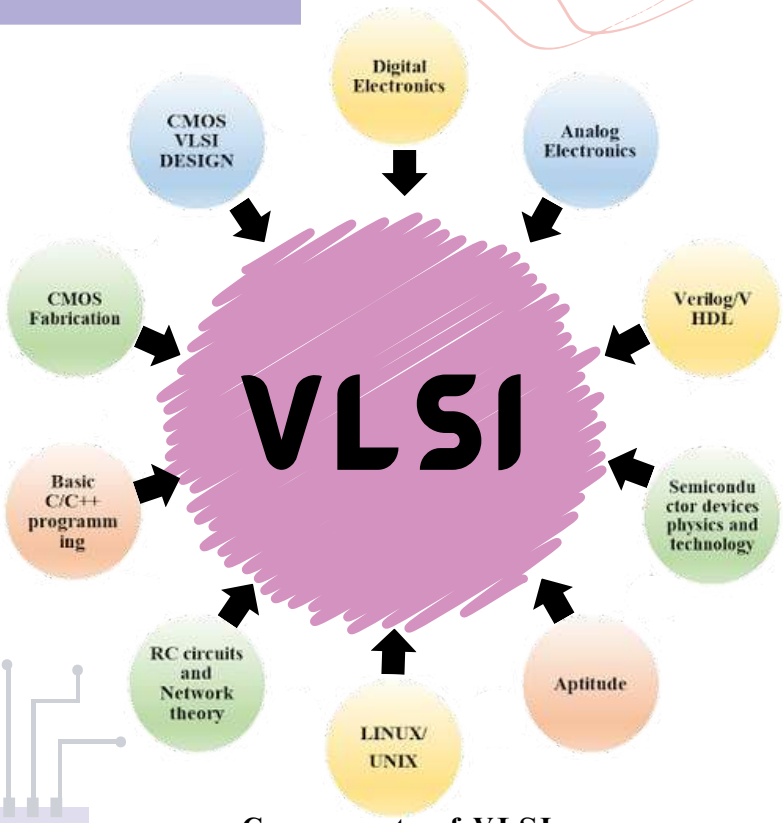
The front-end, akin to an architect, focuses on the chip's functionality and blueprint. Here's a breakdown of key tasks:

- **Conceptualization and Specification:** It all starts with understanding the chip's purpose. Front-end engineers meticulously define its functionalities, performance targets, and operational environment.
- **Architectural Design:** With the purpose etched, the architect lays out the blueprint. This involves defining the chip's core components, their interactions, and communication protocols.
- **HDL Coding**: Hardware Description Languages (HDLs) like Verilog or VHDL come into play. Here, engineers meticulously translate the architecture into a coded representation, defining how the chip operates on a logical level.
- **Functional Verification**: The architect wouldn't build a faulty structure! Similarly, front-end engineers employ rigorous verification techniques to ensure the HDL code accurately reflects the intended functionality. This involves creating testbenches that simulate various input scenarios and validting the chip's behavior.

Back-End Design: Translating Logic to Silicon

The back-end takes the architect's blueprint and transforms it into the physical chip. Here's what goes on behind the scenes:

- **Logic Synthesis:** The verified HDL code is converted into a detailed blueprint (netlist) showing the actual electronic circuits needed.
- **Placement and Routing:** Like arranging furniture, transistors, logic gates, and connections are positioned on the chip for optimal area, power, and signal transmission.
- **Physical Design and Verification:** After placement and routing, the chip's physical layout is checked for errors and adherence to manufacturing rules and performance targets.
- **Fabrication and Testing:** The verified layout is translated into instructions for chip fabrication. Once manufactured, the chips are rigorously tested to meet all specifications.



Components of VLSI

Image Courtesy :-https://techovedas.com/10-vlsi-breakthroughs-of-2023/

Major Companies offer Job Opportunities in VLSI:

1. *Intel Corporation*
2. *Qualcomm*
3. *Samsung Electronics Co. Ltd*
4. *Broadcom Corporation*
5. *ARM*
6. *Advanced Micro Devices, Inc (AMD)*
7. *NVIDIA*
8. *Infineon Technologies*
9. *MediaTek Inc.*
10. *NXP Semiconductors*
11. *Credence*

"The Indian Semiconductor industry is projected to grow significantly, with demands for semiconductor goods expected to reach INR 29,988 billion FY 2025".

JOB OPPORTUNITIES

VLSI offers a plethora of job opportunities in the field of semiconductor design and engineering. From designing integrated circuits (ICs) to testing and verification, VLSI professionals play a pivotal role in developing cutting-edge electronic devices.

Front-End Design Engineers consist of following role :

- **RTL Design Engineer:** Creates the core logic of the chip using Hardware Description Languages (HDLs).
- **System Design Architect:** Defines the overall architecture and functionality of complex VLSI systems.
- **Verification Engineer:** Develops test benches and simulations to ensure the chip functions as intended.
- **IP (Intellectual Property) Designer:** Designs reusable functional blocks that can be integrated into different chips.

Back-End Design Engineers consist of following role :

- **Physical Design Engineer:** Performs placement, routing, and other tasks to create the physical layout of the chip.
- **Logic Synthesis Engineer:** Converts the RTL code into a netlist, a detailed blueprint of the logic gates needed on the chip.
- **Place and Route Engineer:** Optimizes the placement and routing of components on the chip layout for performance and efficiency.

EMERGING TECHNOLOGIES IN VLSI

- **AI-Driven VLSI Design:** Artificial intelligence (AI) is transforming the VLSI design process by automating and optimizing critical tasks. Machine learning algorithms can analyze vast amounts of design data to identify patterns and help engineers make informed decisions. This can significantly reduce design time and improve chip efficiency.
- **Heterogeneous Integration**: This approach combines different materials and technologies onto a single chip. For example, a chip might integrate logic transistors, memory cells, and sensors made from different materials, each optimized for a specific function. This allows for more efficient and powerful chips.

Image Curtesy: https://images.app.goo.gl/8bbBLmLBzcRcLUft8t

- **3D Integration:** Traditionally, ICs have been designed in a two-dimensional (2D) manner. However, 3D integration allows stacking multiple layers of transistors vertically, creating denser and more powerful chips. This technology is still in its early stages of development, but it has the potential to revolutionize VLSI design.
- **Neuromorphic Computing:** Inspired by the human brain, neuromorphic computing aims to create chips that can process information in a similar way. These chips can be more efficient for tasks like artificial intelligence and machine learning.

In early 2020, Synopsys introduced DSO.ai, the first AI application for chip design. Using reinforcement learning, it enhances exploration of design workflows, automating decisions for better, faster, and cheaper semiconductors. In November, Samsung utilized DSO.ai with Synopsys Fusion Compiler, achieving top performance and energy efficiency at an advanced node. This demonstrates the solution's autonomous capabilities, which improve over time with learning technology.

DID YOU KNOW?

AI-related semiconductors could make up 20% of market demand by 2025, according to a report by McKinsey & Company. The report goes on to note that semiconductor companies could capture up to 50% of the total value from the technology stack thanks to AI. Given the opportunities, a number of startups as well as hyperscalers have stepped on to the chip development stage.

Applications of VLSI

- **Consumer electronics:** Smartphones with AI-driven processors, high-resolution cameras, and energy-efficient components have become indispensable tools for communication and entertainment.
- **Scientific research:** High-performance microchips power supercomputers used in scientific simulations, enabling breakthroughs in climate modeling, drug discovery, and astrophysics.
- **Healthcare:** Microchips are crucial in medical imaging devices, genetic sequencing machines, and implantable medical devices, enhancing diagnostics, treatment, and patient care.

AI DRIVEN CHIPS

- **Significance of AI in chip design**

***Ability to optimize the PPA of chips*:** EDA(Electronics Device Automation) tools can help optimize power, performance, and area (PPA). This means the chip is designed to use the least amount of electricity while accomplishing its designated task.

Ability to automate certain chip design tasks: AI can automate chip design tasks such as place route and debug. Now, AI can automate the optimization of place and route tasks with intelligence.

Bridging the gap in chip design talent: With the global boom in electrification, the demand for semiconductor chips is growing. Here, AI tools can help bridge the workforce gap by automating aspects of the tasks that rely upon extensive prior knowledge.

- **Market analysis for AI in chip design**

Marketresearch.biz, a renowned market research firm, recently unveiled an insightful research report focusing on the dynamic Generative AI in Chip Design Market. The report provides an accurate and comprehensive analysis of the long-term prospects of both the global and regional markets.

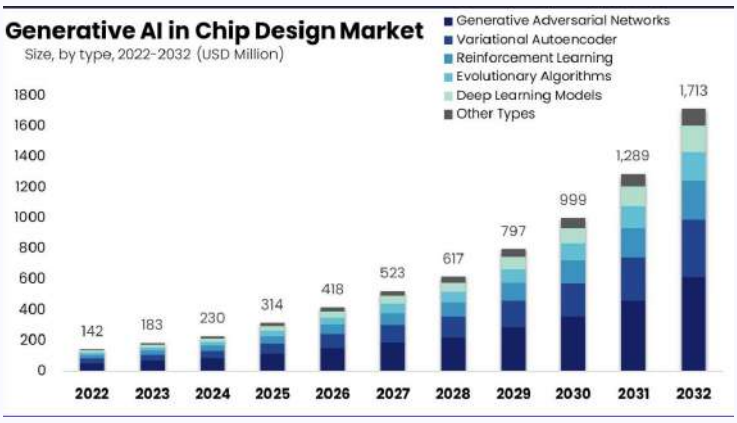


Image Courtesy:-https://www.linkedin.com/pulse/generative-ai-chip-design-market-designing-future-kevin-pat/

- **Reinforcement Learning**

Reinforcement Learning (RL) is revolutionizing Electronic Design Automation (EDA) by optimizing power consumption and streamlining placement and routing (P&R) tasks on printed circuit boards (PCBs). RL fine-tunes circuit parameters to minimize power usage while maintaining performance standards, benefiting applications like mobile devices and data centers. In PCB design, RL automates component placement and interconnection routing, optimizing for factors such as signal integrity and manufacturing cost. These RL-driven approaches accelerate design cycles and improve overall performance compared to traditional methods, marking a significant advancement in EDA efficiency.

- **Electronic Design Automation (EDA) and it's importance.**

Electronic Design Automation (EDA) software, hardware, and services are vital for chip and semiconductor design. With the advent of Artificial Intelligence (AI), EDA has evolved to optimize Power, Performance, and Area (PPA). AI-infused EDA tools streamline simulation, verification, and chip rollout processes, reducing time to market (TTM) and meeting customer expectations. EDA's integration with AI enhances efficiency, enabling designers to create innovative semiconductor solutions that align with market demands. This fusion of EDA and AI marks a significant advancement in semiconductor design, empowering companies to produce cutting-edge devices efficiently and effectively.

Future of VLSI

Quantum Computing in VLSI

An emerging field that combines the principles of quantum mechanics with the technology of VLSI. This intersection presents unparalleled possibilities for processing power and performance.

1) Quantum Machine Learning in VLSI Placement: Quantum computing has shown potential for utilization in VLSI placement problems, where traditionally heuristic solutions such as Kernighan-Lin (KL) are used. A quantum backend generates data for classical algorithms to optimize control parameters, creating a hybrid quantum-classical computing loop.

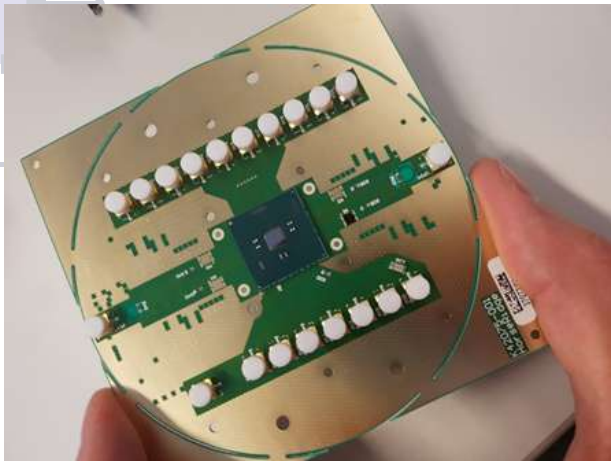
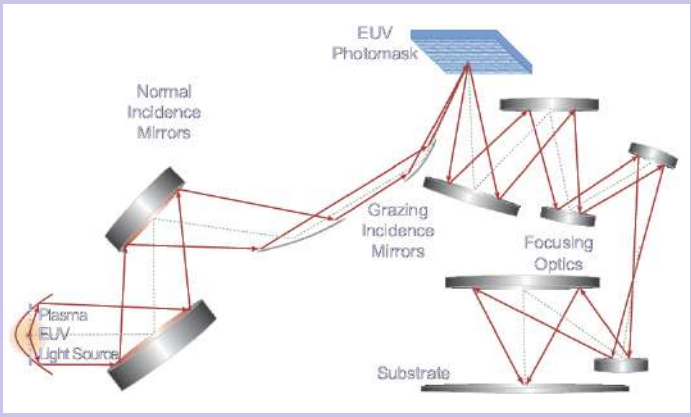


Image Curtesy: https://maker.pro/blog/intels-horse-ridge-chip-and-what-it-means-for-the-future-of-quantum-computing

2) VLSI Architecture for Quantum Computing Interface: A VLSI architecture has been designed to interface with quantum computing structures. This architecture aims to facilitate seamless communication between classical VLSI circuits and quantum processors, allowing the efficient translation of quantum computational results into actionable data for classical systems.

Need of EUV lithography for future of chips

To continue making chips smaller and smaller, we need powerful, accurate machines to manufacture those chips. This where EUV lithography comes in. Which uses EUV light to create intricate patterns on silicon wafers.



Physics behind EUV Lithography

Image Curtesy: https://images.app.goo.gl/kjit2M9ub8FL42Jy5

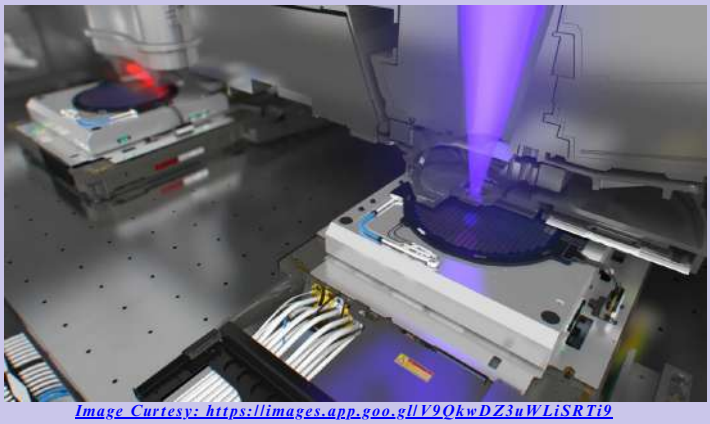


Image Curtesy: https://images.app.goo.gl/V9QkwDZ3uWLiSRTi9

1. **EUV Light Source:** The EUV light source is based on a laser-produced-plasma (LPP) technology. A high-power laser is used to create a plasma, which emits EUV light at 13.5nm wavelengths.
2. **EUV Process:** The EUV process takes place in a vacuum environment because nearly everything absorbs EUV light. The process involves transferring integrated circuit (IC) patterns on a reflective mask to a resist film on a wafer.
3. **EUV in IC Manufacturing:** As of 2023, ASML Holding is the only company that produces and sells EUV systems for chip production, targeting 5 nanometer (nm) and 3 nm process nodes.

GOVERNMENT INITIATIVES FOR VLSI

Make in India Program: The Make in India initiative has been instrumental in promoting the growth of the VLSI industry by encouraging domestic manufacturing and attracting foreign direct investment.

Tata Group initiative 2024: The Tata Group will set up a semiconductor manufacturing plant in Assam's Jagiroad with an investment of ₹27,000 crore.

VLSI Design Conference 2023: With the theme "Semiconductors Driving Disruptive Innovations in Global Digitalization," this conference aims to highlight India's growing capabilities in the VLSI industry[1].

SemiconIndia 2022: At the SemiconIndia conference, multiple agreements were announced to catalyze India's semiconductor ecosystem. This includes MoUs to enable mass production of the "5G Narrowband-IoT-the Koala Chip," designed in India, and the deployment and maintenance of 10 Lakh Integrated NavIC and GPS Receivers.

Design-Linked Incentive (DLI) Scheme: The Indian government announced a DLI scheme to encourage global and domestic investment related to design software, IP rights, etc., from MSMEs and startups. This scheme offers financial incentives and infrastructure support across various stages of semiconductor design for a period of 5 years.

National Policy on Electronics: The Indian government's National Policy on Electronics aims to boost the VLSI industry's growth by leveraging new technologies such as IoT, AI, and 5G, which are expected to drive the demand for VLSI chips.

ECONOMIC IMPACT

With constant push to remake ICs, demand for VLSI engrs is surging

Shivananda Kotechwar

BUILDING A CAREER IN SEMICONDUCTOR - 1

Semiconductor industry in India can be categorised into the following:

- Product companies like Intel, Qualcomm, MediaTek, Texas Instruments, ST, Infineon, Broadcom, Micron
- IP companies like Synopsys, ARM
- Foundries like TSMC, Global Foundries, UMC
- Services companies like HCL, cinfochips, Wipro, Quest Global, Mirafra
- Electronic design automation (EDA) companies like Synopsys, Cadence, Ansys
- Fabless design companies like Saankhya Labs, AlphaICs, Steradian, Auro, Circl, Lightspeed.ai

Production-Linked Incentive (PLI) Scheme: Announced in December 2021, this roughly $10 billion dollar scheme is designed to encourage semiconductor manufacturing in India. It is expected to increase India's share of global electronics manufacturing significantly over the next few years.

MoUs for Semiconductor Production: At SemiconIndia 2022, MoUs were announced to enable mass production of the "5G Narrowband-IoT—the Koala Chip," designed in India, and for the deployment and maintenance of 10 lakh integrated NavIC and GPS receivers.

Modified Electronics Manufacturing Clusters (EMC 2.0) Scheme: This scheme provides financial and infrastructural support for developing electronics manufacturing clusters across India. These clusters can house companies involved in VLSI design and other aspects of the electronics value chain.

Chips to Startup (C2S) Programme: This program focuses on training manpower for the semiconductor industry. It aims to train 85,000 engineers specializing in VLSI design, fabrication, and related fields. This skilled workforce is essential for the growth of the domestic VLSI industry.

These plans are part of a broader strategy to make India a global hub for electronics manufacturing and design, and they represent a significant investment in the future of the VLSI industry.

Growth Projection: India's share of global electronics manufacturing is expected to rise to about 10% in four to five years from the current 3.5%.

Market Value: The worldwide semiconductor industry, of which VLSI is a part, is currently valued at $500–$600 billion and caters to the global electronics industry, valued at about $3 trillion.

Demand Increase: Semiconductor demand in India is projected to increase to $70-$80 billion by 2026 due to the growing demand for digital devices and electronic products.

Global Economic Impact:

Industry Growth: The semiconductor market has boomed, with sales growing by more than 20% to about $600 billion in 2021. It's expected to reach a $1 trillion industry by 2030.

Market Predictions: The global VLSI market is estimated to be worth USD 662.2 billion in 2023 and is predicted to grow to USD 971.71 billion in 2028, at an 8% compound annual growth rate (CAGR).

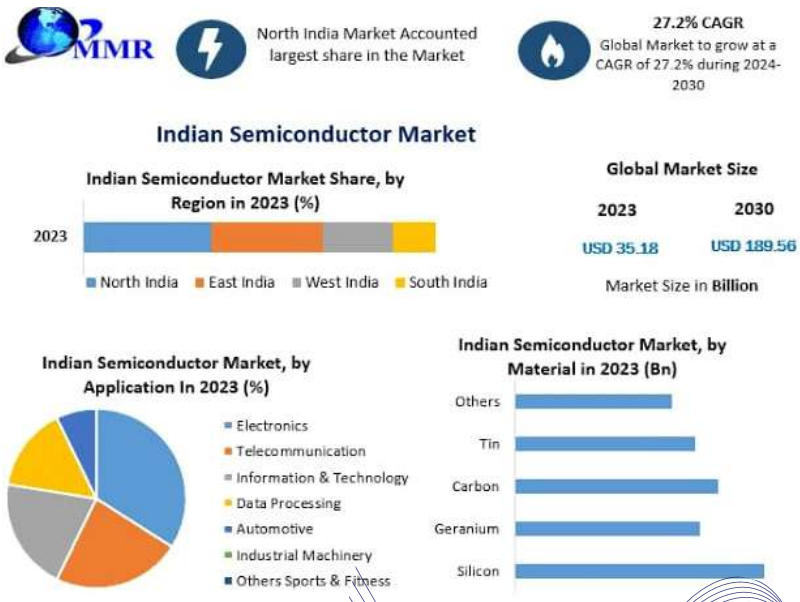


Image Courtesy :- https://www.maximizemarketresearch.com/market-report/indian-semiconductor-market/14504/

Exploring a Career in VLSI: A Journey into Semiconductor Design and Chip Manufacturing

This alumni spotlight, delve into the realm of VLSI, exploring the intricate landscape of semiconductor design and chip manufacturing.

SUYOG PATIL

BATCH 2016
VLSI ENGINEER - DFT DOMAIN
AS SR. ENGINEER AT QSILICON INNOVATIVE SOLUTIONS

Hello friends! I am Suyog from the 2016 EXTC Batch. I have done my Masters specializing in VLSI and Embedded Systems and currently working as a DFT Engineer also know as "Design for Test Engineer". Usually, people mistake DFT with Discrete Fourier Transform or hearing of the Test Engineer term relate it to engineers holding tester probes on the Silicon Chip Assembly Line. None of that is true, actually it is related to introducing certain extra logic inside the chip which enables us to find out faulty devices after the manufacturing process. Don't bother yourself much about it, we will get back to it in sometime. In line with the theme of our magazine "VLSI", I will try to shed some light on my experiences of VLSI Industry and the journey so far. Let's get started!

Post my Graduation from VCET through the GATE exam I got an admission into IIIT-Delhi (there's a 3rd I !!) for a Master's where they had Industry focused curriculum. Our Bachelor's Degree is a Generalized Degree covering all the basic domains while Master's usually caters to a certain specialization. The curriculum focused on VLSI processes and Embedded Systems architecture thus making one ready with the basic skillset required by the industry. Let's discuss more on the insights of what is taught in such master's courses which is sought by industry.

We know that the electronic chips used in instruments around us are all majorly made up of CMOS Transistors in huge numbers (that's why the name VLSI). In reality the VLSI industry also caters to the LSI, MSI circuits and even Device Level Physics study. We can broadly consider the following major levels in VLSI domain: Device Level (focusing on the MOS level Device Physics and Research), Circuit Level (Digital/Analog/Mixed Signal designs) and System Level (dealing with the interactions of all the circuits of the system). So, majorly the courses deal with each of these levels. Courses like "**Analog CMOS Design**" and "**Digital VLSI Design**" cover the Device Physics part with basic circuit design, while "**Mixed Signal Design**" combined both. "**Computer architecture**" course brings study of traditional pipelined architecture System level Design. Now-a-days it is complimented with the study of "**Heterogenous Platforms**" (CPU + GPU + FPGA) which are the latest buzz in System Level Design.

But you may say what exactly happens in a VLSI Chip design cycle in Industry and where does that term DFT fit into? The cycle is called as "VLSI Design Flow" (we had a course on this...) and it starts from the C/C++/Verilog/VHDL based system design code, which is converted into CMOS gate-based logic and then optimized to create a Physical layout for fabrication. Each of this step is a domain in itself and people specialize in them by acquiring the necessary skills. DFT logic is like a diagnosis circuit added inside the chip which helps us to find out the manufacturing defects. The Silicon chip manufacturing process has a reasonably high failure rate and companies cannot afford to roll out defective chips in market without proper scrutiny. Hence if you see the actual cost of

manufacturing chips in the market without proper scrutiny. Hence if you see the actual cost of manufacturing a chip, around 60% is spent on testing and verification!! DFT and Verification Engineers file for patents if they devise a method to reduce even ~3% of this testing cost because for companies it saves millions which is profit for them. Money drives innovation literally!

To understand the VLSI industry flow, let's take an example of a mobile processor chip design your company is handling. In this chip, you would have systems like CPU, GPU, camera controllers, WiFi and Bluetooth controllers, display controller, DSP, video codec, audio codec, a good modem, etc. For each of these, you will have the design code which your Design engineers will synthesize into CMOS-based logic. On top of this, the DFT engineers will introduce their logic to support testability. The Physical design engineers will then optimize this design to meet the required chip specifications for example the CPU should work at 3.2GHz and also fit into the prescribed silicon area. This optimized layout is then sent to the fabrication company, meanwhile parallelly your DFT and Verification engineers need to be ready with their generated test patterns which they can use to check and sort out defective pieces. Mind you nothing is free in the industry; the failed chips are analyzed for failure reasons and then either the manufacturing company or the design company has to pay for the failed parts based on the analysis.

I had the opportunity to work on multiple chips spread out over different technology nodes. For us (DFT engineers), we always need to implement and enhance our designs and flow to cover maximum corner conditions in our test patterns. The increasing size of the designs and small execution timelines add to the complexity of the process. The major goal is to generate and deliver effective test patterns covering most of the known corner cases. For example, the chip under test is subjected to different voltages and temperature conditions to mimic the original use-case scenarios. If any failures occur then we may need to analyze and update the pattern or sometimes in design bug scenarios we take the learning in future versions of chip release.

You might have noticed lately the emphasis put by the government on expanding the VLSI presence in India and their focus on creating a skilled talent pool. Your skills are the most important for you to grow in the industry, your degree has a secondary role there. Good colleges will help you with a head-start in the industry, but if you don't get into one then check what skillsets are required by the industry. One trick to know what skills are sought is to check out the job description of various entry-level engineering posts, you will get to know the trend from there. Every company looks for a person who has a logical approach to solving an issue, for always you will not get the same problem again in this changing world. With the onset of AI and automation, the requirement of VLSI engineers to support the revolution will always be there. I am too learning many things and acquiring new skill sets, who knows somewhere down the line I might be in some other work than DFT!

Friends, with this I think I should end as GenZ usually do not like the continuous blabber of "Gyan" and that too from a millennial . All the Best everyone,

Suyog Patil
Alumni- EXTC, VCET

KAVITA DESHPANDE

BATCH 2013
SENIOR ASSOCIATE~PROJECTS AT COGNIZANT |
WORKED AS TECHNICAL LEAD AT KPIT

The Software-Defined Vehicle

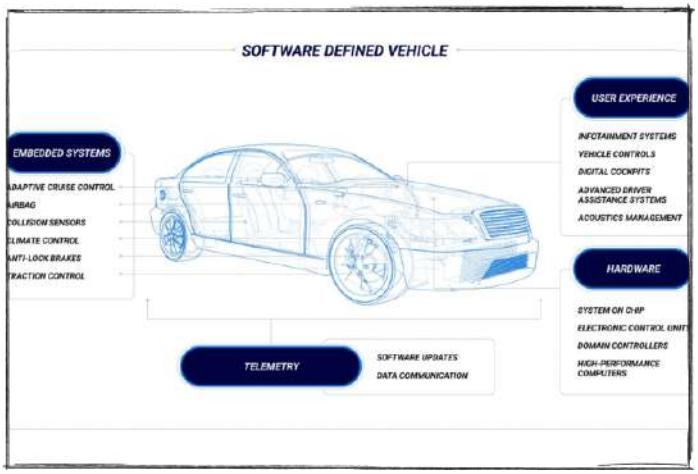
Many car drivers expect their vehicles to be fully integrated into their digital lives. In addition, new connectivity, automation, and personalization features will be increasingly implemented with software in the future. While in the past the customer's experience of a car was primarily defined by hardware, software is now taking on a much more important role. This trend of software massively shaping the customer experience and in some cases even the specification of the hardware is referred to as the "software-defined vehicle" (SDV). This evolution not only affects development and operation, but also makes new business models and types of collaboration possible.

A Software-Defined Vehicle is any vehicle that manages its operations, adds functionality, and enables new features primarily or entirely through software.

Software-Defined Vehicles are the next evolution of the automotive industry. They are the foundation of many other advancements, including self-driving and connected cars.

Software-Defined Vehicle Architecture

Software-Defined Vehicles (SDVs) feature intricate architectures with four layers: User Applications directly engage drivers and passengers, facing challenges of compatibility and integration. Instrumentation manages vehicle functions like ADAS, requiring seamless sensor integration and real-time processing. Embedded OS, the core system, tackles security and flexibility hurdles. Hardware poses a unique challenge due to tight software-hardware coupling, mitigated by agile, modular development. Virtualization separates software from hardware, enabling smoother updates and performance optimizations.



Software Defined Vehicles and Vehicle-to-Everything

Software-defined vehicles prioritize connectivity, enabling over-the-air updates and real-time information for drivers. They are integral to Vehicle-to-Everything (V2X) technology, facilitating constant two-way communication with surroundings. V2X utilizes high-bandwidth, low-latency wireless connectivity like 5G to enhance safety and enable driver services, aligning with smart city developments. SDVs streamline V2X integration through software stacks and standard-based communication methods, acting as hubs for data exchange. This technology empowers vehicles to leverage urban IoT sensors and contribute to central repositories, enhancing safety and providing driver services like automatic payments for restricted urban areas.

Software Defined Vehicles and Autonomous Vehicles

Autonomous vehicles depend on sophisticated software models, developed through intensive AI/ML processing on powerful supercomputers, to predict road behavior. While a variety of sensors, including cameras, radar, and LiDAR, provide input, it's the software's ability to interpret this data that enables autonomy. SDVs streamline this process by centralizing core driving functions like acceleration and braking, integrating them via interconnected software on a central computer. This architecture not only facilitates seamless control but also allows for regular software updates to incorporate new capabilities and safety improvements. As the technology evolves, the reliance on fixed hardware platforms diminishes, enabling dynamic upgrades to meet evolving needs. Ultimately, the emphasis on software in autonomous driving systems underscores the critical role of ongoing innovation and adaptation in achieving fully self-driving capabilities.

Software Defined Vehicles and Cybersecurity

To compromise vehicles without connectivity, threat actors need physical access—they need to be near the car when keyless entry is invoked or be in a location with both the car and its keys in the vicinity. For deeper levels of compromise, they would need to enter the vehicle to connect to the diagnostics port.

With an SDV, these functions could be accessed remotely, similar to the malware attacks perpetrated on personal devices and corporate systems. Although there have been no publicized incidents of this occurring (except for controlled demonstrations), the mission-critical nature and safety requirements of road vehicles mean that a breach could be more immediately serious than the theft of even bank details: A moving car suddenly losing its ADAS functions because of a cyberattack could be life-threatening. A compromised self-driving vehicle could be turned into a weapon.

Vehicle software must implement proactive protection systems against cyberattacks like corporate network systems. Cybersecurity solutions can recognize and nullify existing known attacks and detect behavior that could be a previously unseen attempt to compromise systems. With SDVs employing powerful computing hardware, this can be leveraged to run AI-enhanced cybersecurity, keeping vehicles secure and their occupants safe.

DEPARTMENT

ACTIVITIES AND ACHIEVEMENTS

MEET OUR DEPARTMENT

Dr. Amrita Ruperee
Ph.D. (Wireless Communication)

Area of interest:
Wireless Communication

Dr. Vikas Gupta
Ph.D. (EXTC)

Area of interest:
VLSI, Signal Processing, Digital Communication, Satellite & Radar Communication

Dr. Sunayana Jadhav
Ph.D. (Electronics)

Area of interest:
Wireless Networks

Ms. Shaista Khanam
M.E. (Electronics) (Ph.D Pursuing)

Area of interest:
Microprocessor and Microcontroller, VLSI

Ms. Shraddha Gosavi
M.E. (EXTC)

Area of interest:
Speech Recognition, Optical Fiber Communication

Ms. Sandhya Supalkar
M.E. (Electronics)

Area of interest:
Image Processing, VLSI

Ms. Ashwini Katkar
M.E. (EXTC) (Ph.D Pursuing)

Area of interest:
Computer Networks, Optical Communication

MEET OUR DEPARTMENT

Ms. Neha Gharat

M.E. (EXTC) (Ph.D Pursuing)

Area of interest:
Image Processing, Microwave

Ms. Ekta Naik

M.E. (Digital Electronics)
(Ph.D Pursuing)
Area of interest:
Neural Networks

Ms. Trupti Shah

M.E. (Electronics)
Area of interest:
Image Processing

Mr. Sandeep Pawar

M.Tech. (EXTC)
Area of Interest:
Antenna Design

Mrs. Bhagyashree Rane
Lab Technician

Mrs. Diksha Save
Lab Technician

Mrs. Madhu Lade
Lab Technician

Mr. Prakash Bhobhate
Peon

Mr. Sudhir Patil
Peon

DEPARTMENTAL EVENTS

The **IETE-SF** hosted a seminar titled **'Opportunities in Core Engineering'** on **September 11, 2023**. The seminar provided insights into the workings of the oil and gas sector, covering aspects such as upstream, midstream, and downstream processes. It also emphasized the abundance of opportunities in this field, particularly at companies like **HLS** and **Schlumberger,** and also addressed salary expectations, showcased visuals of rig structures, and discussed the pros and cons of working in the oil and gas industry. The event aimed to inspire students from diverse engineering disciplines.

The **IEEE-SB** and **Texas Committee** united organized an visit, at **A.D. Jadhav Kanya Vidyalaya, Vajreshwari** on **October 19, 2023**, to unveil a groundbreaking **"STEM"** initiative focused on delivering hands-on education in electronics and robotics. The program covers essential topics such as Ohm's Law, series and parallel resistance, basic Arduino programming, and the introduction of Robotics Systems Learning Kit (RSLK) bots. Participants engage in designing circuits incorporating series and parallel resistances and learn basic Arduino programming, including exercises like the "**Blink**" code. The initiative culminates with participants assembling, programming, and testing their own robots using the **"RSLK"** bots. The goal is to provide a comprehensive understanding of electrical engineering principles and the diverse applications of robotics while nurturing a passion for STEM disciplines.

The **"IETE-SF"** led to the organized engaging event titled **"VLSI Design"** on **October 20, 2023**. The purpose of this webinar was to introduce students to VLSI designs flow from concept to silicon – exploring career pathways and opportunities. The webinar surrounded around covering the frontend and backend of it. Further, the talks of career opportunities captured the space and concluded with an interactive Q&A session. Participants engaged in a lively discussion, seeking clarification on topics discussed during the session.

DEPARTMENTAL EVENTS

On **20th February 2024**, **IETE-SF** organized an amusing webinar named "**System on Chip Design**". The purpose of this webinar was to introduce students to the SoC design industry and EDA industry. Several methods were discussed in it, like verification being one of them. The difference between the **ASIC** and **FPGA** was made understood. The architecture and the job market was also elaborated. Attendees engaged in a lively discussion, seeking clarification on topics discussed during the session.

On the auspicious occasion of **Engineer's Day** , **September 15th 2023**, the "**ANVESHAN 2023"** event took place at Vidyavardhini's College of Engineering and Technology the guest for the event was **Mr. Timir Doshi**. This event was a collaborative effort between the **IEEE-SB** and **IETE-SF**, under the esteemed guidance of **Dr. Amrita Ruperee, Dr. Sunayana Jadhav** and **Ms. Shaista Khanam.** ANVESHAN aimed to bridge the gap between local industries and students by providing a platform for companies to exhibit their products and services. The event attracted a substantial response, with more than 15 companies participating and showcasing a diverse array of offerings, ranging from technology solutions to surveillance and home decor.

DEPARTMENTAL EVENTS

From **2nd January 2024** to **12th January 2024**, the Department of Electronic and Telecommunication Engineering in collaboration with **IIT Bombay** organized a Student Development Program on **"Digital System Design & Verification"** using "*CPLD* (Krypton Board)". The workshop was conducted by **Dr. Sunayana Jadhav** & **Ms. Sandhya Supalkar**. The objective of this event was to understand the work of Quartus Software and various types of adder as well as combinational circuits & BCD addition.

The Short Term Training Program (STTP) and the Student Development Program (SDP) on **"Industry 4.0: Paradigm Shift in Technology"** was successfully conducted from **26th June 2023** to **1st July 2023** at the VCET Seminar Hall. The program aimed to familiarize faculties and students with the latest advancements in Industry 4.0 and its transformative impact on various industries. With the participation of eminent speakers from academia and industry, along with hands-on sessions and an industrial visit to the **"Amul factory"**, the program provided a comprehensive learning experience to the students.

CAREER GUIDANCE

A seminar on **'Career Guidance- Your Guide to Effective Placement Strategies'** was organized on **September 14th, 2023**. The speaker of this interactive seminar was alumni **Mr. Lavesh Salaskar,** Zeus Learning and **Mr. Kushal Raut**, LTI. The objective of the seminar was to provide the students with interview excellence, current job market trends, industry connections, job search strategies. This seminar was organized by the Department in association with **Training and Placement Cell of VCET**. Lavesh and Kushal extended their guidance to students interested in various domains, including Network and software engineering.

"Navigating Career Opportunities in Telecomm Networks"

The webinar was organized for TE and BE students of department on **28th March 2023**. The speaker for the event was alumni **Mr. Umang Waghela**, a Software Engineer at Hughes Networks Systems. This informative webinar was organized by the "**IEEE-SB"** of the EXTC Department in association with the **Training & Placement Cell.** The webinar focused on current career opportunities in the Telecom network sector, providing valuable information to students. They received insightful acknowledgement to their queries about pursuing further studies in the field.

INDUSTRIAL VISITS

The **IETE-SF** organized an industrial visit to **Aczet Pvt. Ltd, Vasai** on **February 15, 2024**. 53 Students along with 2 faculties **Ms. Shaista Khanam and Ms. Sandhya Supalkar** were present for the visit. The industry is a high-tech manufacturer providing comprehensive solutions for a wide range of weighing scales, laboratory balances, STENT weighing microbalances, laboratory testing equipment, jewellery balances, jewellery machinery, industrial scales, XRF, and laser applications. This visit provides students a chance to learn practically from theoretical knowledge through interaction, working methods.

On **2nd April, 2024**, Electronics & Telecommunications and Mechanical Department in association with **IETE-SF**, organized an industrial visit to **Adani Power Station, Dahanu**. 47 students from the SE, TE, and BE, as well as faculty members, **Mr. Mukund Kavekar, Mrs. Ashwini Katkar** and **Ms. Neha Gharat** were present for the visit. The company has a coal based thermal power plant which has an installed capacity of **500 MW (2x250 MW).** The actual Power Plant and model was explained in detail. The company focuses on preventing emission of harmful gases into the environment.

Staff Achievements

AS REVIEWERS

- Dr. Amrita Ruperee and Dr. Sunayana Jadhav were invited as Session Chair National Conference on Role of Engineers in Nation Building (NCRENB)-2024, at Viva Engineering College, Virar.
- Dr. Amrita Ruperee is a Reviewer for the International Journal of Communication Systems, Wiley Publication, and a Reviewer for the Hindawi portfolio of journals. She was also a Judge for the Jana Kalyan Hackathon, TCET, Mumbai.
- Dr. Vikas Gupta was invited as a guest of honor at the Oscillation event at ACE Techfest, invited as session chair and panelist EMPERA 23rd at BITS Pilani Campus, Hyderabad, invited as Session Chair at Multicon, ICCCDS'24 INTERNATIONAL conference at TCET Mumbai, invited as session chair at ICDLAI-2024 organized by Bikaner Technical University in association with Springer and invited as a Subject Expert for UGC interviews held at TCET Kandivali Mumbai. He also visited facilities of the Semiconductor Design Research Lab, Siemens, and the Data Science Centre of Excellence of PEC, Chandigarh.
- Dr. Sunayana Jadhav was a Judge for the AVISHKAR 2023 competition and a Judge for Science Fest, St. John Campus, Palghar.

PATENT PUBLISHED

- Dr. Sunayana Jadhav as an inventor published a patent titled" Smart Saline Assistance System" with applicants Mr. Sanjay Lohar, Mr. Harsh Dodiya, Mr. Amey More, and Mr.Yash Barot on 8th September 2023.
- Ms. Trupti Shah as an inventor published a patent titled" Smart Attendance System" with applicants Dr. Sunayana Jadhav, Ms. Shaista Khanam, Mr. Mayank Patil, Mr. Omkar Joshi, Mr. Chandan Thakur and Mr. Manthan Patil on 9th February 2024.

PAPER PRESENTED/ PUBLISHED

- Dr. Vikas Gupta presented a paper at the 66th Annual IETE Convention(AIC) Conference, Pune,
- Dr. Vikas Gupta presented a paper at ICDLAI-2024 organized by Bikaner Technical University in association with Springer.
- Ms. Shraddha Gosavi, Ms. Sandhya Supalkar and Ms. Ekta Naik have published a paper with the title" Intelligent Assistance for Smart Shopping" at the International Journal of Engineering and Management Research; Volume-13, Issue-4 (August 2023).
- Ms. Ashwini Katkar has published a paper with the title "Assessing Molecular Throughput and Efficiency through Simulation in Diffusion-Based Molecular Communication" at the Indian Journal of Science and Technology; Volume: 17, Issue: 6, (2024).
- Ms. Trupti Shah has published a paper with the title "AutoProc - AI Based Automated Exam Proctoring System with Test Score Analysis" at the EAI International Conference on Computational Intelligence and Generative AI organized on 24th and 25th March, 2024 at Guntur, India.

BOOK/BOOK CHAPTER PUBLISHED

- Ms. Ashwini Katkar published a paper titled " Investigating the Impact of Distance on the Reception in Molecular Communication" in the chapter named "Intelligent Computing and Networking" with the publisher Springer in August 2023.
- Ms. Neha N. Gharat published a paper titled "Source Location Privacy Protection Algorithms in IoT Networks: A Survey" in the chapter named "Soft Computing for Security Applications" with the publisher Springer.

WORKSHOP/ TRAINING CONDUCTED

- Ms. Shaista Khanam and Ms. Trupti Shah were invited as a Resource Person for the FPGA workshop, at RGIT, Mumbai.
- Ms. Shaista Khanam was invited as a Speaker for Exploring FPGA Design with Xilinx Software, at St. John CoE.
- Ms. Ashwini Katkar conducted a session in the training program of the design team of company Parle Global Pvt Ltd, Vasai.

STTP/FDP ATTENDED

- Dr. Amrita Ruperee, Dr. Sunayana Jadhav, Ms. Shaista Khanam, Ms. Shraddha Gosavi, Ms. Sandhya Supalkar, Ms. Ashwini Katkar, Ms. Neha Gharat, Ms. Ekta Naik, and Ms. Trupti Shah attended NPTE:AICTE Approved FDP on "Accreditation And Outcome Based Learning".
- Dr. Amrita Ruperee, Dr. Sunayana Jadhav, Ms. Shaista Khanam, Ms. Shraddha Gosavi, Ms. Sandhya Supalkar, Ms. Ashwini Katkar, Ms. Neha Gharat, Ms. Ekta Naik, and Ms. Trupti Shah attended ISTE approved one week STTP on "Innovative and Creative Approaches for Teaching and Research".
- Dr. Vikas Gupta was invited to attend NEP 2020 Sensitization two days workshop organised by UoM
- Dr. Sunayana Jadhav, Ms. Shaista Khanam, Ms. Shraddha Gosavi, Ms. Sandhya Supalkar, Ms. Neha Gharat, Ms. Ekta Naik and Ms. Trupti Shah attended ISTE approved two week STTP on "Exhilarating socio-human life using Deep Learning" .
- Ms.Shaista Khanam and Ms. Sandhya Supalkar attended AICTE sponsored ATAL FDP on " Semiconductor Digital System Design and Verification".
- Ms. Shraddha Gosavi & Ms. Trupti Shah attended ISTE-STTP/FDP on "Cultivating The Future of Healthcare with Generative AI".
- Ms. Neha Gharat attended AICTE sponsored ATAL FDP on "Information Security Management: A Practical Approach".

STUDENT ACHIEVEMENTS

Mr. Mayank Patil, Mr. Omkar Joshi, Mr. Chandan Thakur and Mr. Manthan Patil **Published a Patent** for **'Smart Attendance System'**.
Also, won Third Price in **Hardware category.** at Datta Meghe College of Engineering.

Mr. Mayank Patil, Mr. Omkar Joshi, Mr. Chandan Thakur and Mr. Manthan Patil won Consolation Prize in the 48 hours Hardware Hackathon 2024 category for Innovative **'Saline Infusion Technology'**.

The team has also presented VCET for Zonal Round of Avishkar'24.

Ms. Rashmi Mote, Mr. Omkar Naik, Ms. Devisha Shetty and Mr. Atharva More won Third Prize in the **48 hours Hardware Hackathon 2024** category for **'Water Surface Cleaning Bot'** at Thadomal Shahani College of Engineering and Technology

DEPARTMENTAL TUG OF WAR TEAM

DEPARTMENTAL BADMINTON TEAM

- Manthan Patil, Vijay Patil, Rohit Arnalkar, Sumant Ganiga, Omkar Naik, Sahil Mhapadi, Omkar Joshi and Ankit Pandey won the first prize in departmental Tug of war.
- Varun Parab, Bhargavi Atre, Rashmi Mote, Vikas Soman, Devisha Shetty and Aryan Kore won the 1st prize in Mixed Doubles Badminton.
- Varun Parab (TE) won the 1st prize in boys single Badminton.
- Varun Parab (TE) & Aryan kore (TE) won the 1st prize in boys doubles Badminton.
- Bhargavi Atre (SE) won the 1st prize in girls single badminton.
- Bhargavi Atre (SE) and Disha Pote (SE) won the 1st prize in girls doubles Badminton.
- Varun Parab (TE) and Devisha Shetty (TE) won the 1st prize in Mixed Badminton.
- Manthan Patil, Vijay Patil, Rohit Arnalkar, Sumant Ganiga, Omkar Joshi, Rohan Vishwakarma , Pawan Singh and Ankit Pandey has secured runner-up position in class-wise Tug of war.
- Sahil Gorivale (TE) won the Runner-up position in the "Choose Your Anime" competition at Litfest'24 conducted by Literati Club
- Omkar Shelke (TE) won the first prize in Boys Single Carrom

ZEAL'24

- Prapti Gowari, Krutiksha Lonkar, Sakshi Padalkar and Tejaswini Tambe, in collaboration with SE IT, won the first-place victory in group dance at Zeal 2024.
- Dhanashree Tandel (BE) won Second prize in Antakshari.
- Omkar Shelke in collaboration with Shruti Jadhav (TE CSE) has secured the runner-up position in Mixed Doubles Carrom

CAMPUS PLACEMENTS 2024

Congratulations

SHRADDHA KOBNAK

Placed in Vodaphone Idea

MAYANK PATIL

Placed in Bristlecone

GATE QUALIFIED

Lavesh Salaskar

Batch-2023

Riddhi Garudkar

Batch-2024

Higher Studies

Pratik Pandit

Batch- 2017-18

University Of Mumbai

Master of Technology in Computer Engineering

Janhavi Jadyar

Batch- 2022-23

University of Lambton, Canada

Advanced Project Management and Strategic Leadership

Ashwin Nair

Batch- 2022-23

Brunel University, London

MSc Data Science and Analytics

Varad Marathe

Batch- 2022-23

University College Cork, Ireland

MSc Business Analytics

Toppers

A.Y. 2022-23

B.E Toppers

1st	Kushal Raut	9.38
2nd	Riddhesh Vanjara	9.35
3rd	Harsh Dodiya	9.34

T.E Toppers

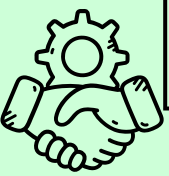
1st	Vijay Patil	9.25
2nd	Nikhil Kargatia	8.92
3rd	Dhanashree Tandel	8.77

S.E Topperss

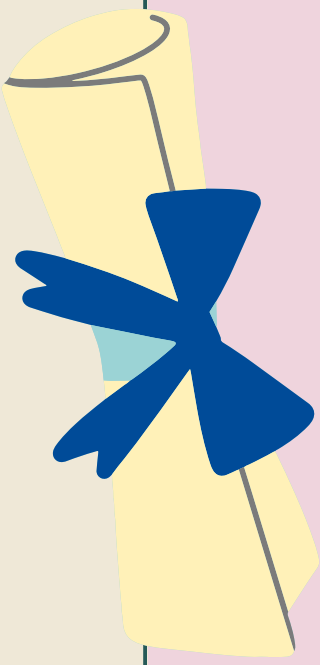
1st	Harsh Shimpi	9.09
2nd	Rashmi Mote	8.57
3rd	Kaushal Wadekar	8.32

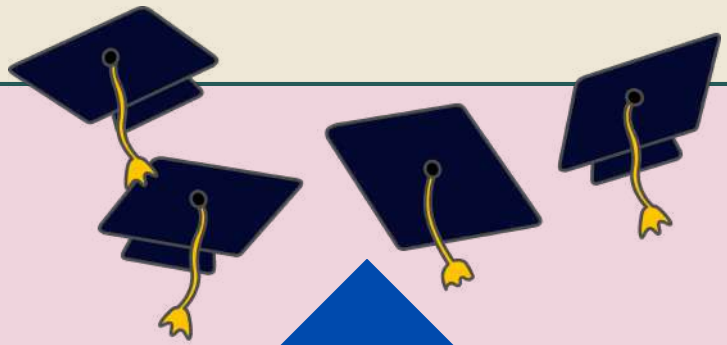
MOU DETAILS

SR. No	NAME OF COMPANY
1	EVERGREEN ENGINEERING CO. PVT LTD
2	SECURIZEN SYSTEMS PVT. LTD
3	WHIRLYBIRD ELECTRONICS PVT LTD,
4	FOX DOMOTICS PRIVATE LIMITED
5	SMART VISION TECHNOLOGIES
6	OM TECHNICAL SOLUTIONS
7	EUROPOWER
8	IIOT EXPERT
9	NN TECHNOLOGY SOLUTIONS
10	LOGIQ EMBEDDED SYSTEMS INDIA PVT LTD
11	TROPICAL ELECTRONIC EQUIPMENT CO
12	PROCESS PRECISION INSTRUMENTS (PPI)



ALUMINI CORNER





Lets meet Mansi Patil, a seasoned professional in the realm of SoC, a graduate with a MS in Electrical and Computer Engineering from Portland State University.

MS. MANASI PATIL

BATCH-2019

SILICON DESIGN ENGINEER AT ADM

1.How do you envision the evolution of silicon design engineering over the next decade?

As per Moore's law, we can observe that the process technology nodes keep shrinking, this helps pack a large number of transistors in a given area and improve the performance of a chip. So, there is going to be development of this process technology further until it reaches its limits.

2.How was your experience in the dream company of many SOC engineers i.e. 'Intel'? and how was the work culture over there?

My experience at Intel has been wonderful, as it was my first company to work as a design engineer. To work on Intel's next-gen processor projects which will eventually make their way into various laptop devices and enable a lot of customers to be able to take advantage of them to improve their workflow experience is a great feeling. The culture at Intel is very friendly and welcoming, and it was challenging and motivating at the same time.

3.Can you describe a time when you had to troubleshoot a complex design issue, and what steps you took to resolve it?

I have experienced this multiple times, while working at Intel as well as AMD. Very recently, I was verifying my design logic with the help of Systemverilog Assertions, and I found a critical bug in a parallel block. Upon encountering this issue, I followed some basic steps which include referring to the Design Specification to confirm if the issue is legitimate, then finding the root cause of the issue and providing a probable solution to the corresponding design engineer and tracking the issue until it gets fixed.

4.How does knowing the Python language help in a design engineer role? And what other software skills are needed for this?

In my experience, I have mostly seen Python or Perl being used as scripting languages across the hardware domain, and knowing these scripting languages is a preferred skill. Automation is achieved using a scripting language, and it helps to build scalable logic which can be implemented in an effective manner as we transition from one project to another.

5.What made you inspired to be a design engineer after your master's in electrical and computer engineering?

I have always been fascinated by how computers work, which is why I decided to pursue a master's degree to gain in-depth knowledge on this subject. As I learned more about the involved topics and completed multiple projects across my coursework, I came to realize that I have an interest in programming and logic implementation, and this inspired me to pursue a career as a design engineer.

6.You have been a design engineer at Intel and are now working with AMD, Which skill sets have you developed and what courses have you done to upgrade your profile? Can you give an overview of what is LEC and SVA exactly?

The most fundamental skill required for a hardware engineer is knowledge of SystemVerilog/Verilog language. I have also picked up some scripting skills along the way. Apart from this, courses that provide knowledge on Computer Architecture and verification using SVA/ UVM can help upgrade a person's skill set and develop their profile.

Without going into much depth, LEC stands for Logic Equivalence Check. These checks are done to confirm that the implemented design logic in SystemVerilog matches with its corresponding logic in the gate-level netlist.

SVA stands for SystemVerilog Assertions. These are checks written as SystemVerilog code statements to verify that the logic implemented by the Design Engineer matches with the Design Specification.

7.Is it possible that one can take only certifications instead of a master's and still be a design engineer?

Taking up relevant certification will help strengthen your profile but a higher education in a particular major would elevate it more and give you more streamlined knowledge and exposure to the opportunities in the job market.

8.What are the differences you observed between the environments while pursuing the undergraduate degree and the master's degree?

Bachelor's degree introduced me to the options I could explore for my career. Whereas master's degree was more focused on a selected major. Masters provides an in-depth knowledge in the courses that you can pick as per your interests.

Introducing Varsha Parab, a Senior Software Engineer at Tech Mahindra, bringing extensive expertise to the forefront of technological innovation. Join us as we delve into Varsha Parab's journey, exploring her profound contributions to the dynamic field of Software Engineering.

MS.VARSHA PARAB

BATCH 2016

SR.SOFTWARE ENGINEER AT TECH MAHINDRA

1. Can you share an example of a project you led at Tech Mahindra that showcases your expertise?

Once a Tech Mahindra client came up with a requirement to migrate a feature completely. The old code was written in Mason and Perl. My expertise in easily adapting to any programming language made me understand the existing code very quickly. As a result, Higher and Lower level design documents were prepared in detail and overall migration was also completed well in advance.

2. Can you describe your journey from a system engineer at Infosys to a senior software engineer at Tech Mahindra?

As a System Engineer at Infosys, I started as a Java Developer. Later at LTI, I tried to learn and adapt emerging technologies along with certifications e.g. AWS Cloud Practitioner and AWS Developer Associate. Similarly at Tech Mahindra, learned a few Client-specific UI technologies. As a result, I work today as a Full Stack Developer and also got an opportunity to lead a couple of projects.

3. What technical skills do you think are most valuable in transitioning between these companies?

Proficiency in programming languages such as Python, Java, JavaScript, C++, etc., depending on the specific requirements of the new company. Understanding of web technologies including HTML, CSS, JavaScript, and frameworks like React, Angular, or Vue.js, depending on the company's tech stack. Familiarity with cloud platforms such as AWS, Azure, or Google Cloud, and services like EC2, S3, Lambda, etc., as many companies are migrating their infrastructure to the cloud. All these skills can vary depending on the nature of the roles and industries involved, but possessing a strong foundation in these areas can facilitate a smoother transition between companies in the tech sector. Additionally, adaptability, continuous learning, and effective communication skills are also crucial for success in any new environment.

4. How do you prioritize tasks and manage deadlines when juggling multiple projects?

Prioritizing tasks and managing deadlines when juggling multiple projects can be challenging but achievable with the right strategies. Begin by making a comprehensive list of all tasks associated with each project. Prioritize tasks based on their importance and urgency. Establish realistic deadlines for each task and project. Ensure these deadlines align with the overall project timeline and goals. Divide larger projects into smaller, manageable tasks. This makes it easier to prioritize and track progress. Avoid burnout by taking regular breaks and managing stress. Practicing mindfulness or relaxation techniques can help you stay focused and productive.

5. How do you ensure that your team's skills remain relevant with the rapid evolution of technology?

Encourage and provide resources for employees to upskill and reskill. This can include training programs, workshops, online courses, conferences, and certifications. Regularly assess emerging technologies relevant to your industry and projects. This can involve reading industry publications, attending seminars, and participating in professional networks. Encourage cross-training and knowledge sharing among team members. Provide constructive feedback and recognition for learning and skill development efforts. Acknowledge and reward team members who actively seek out opportunities to enhance their skills and contribute to the team's success.

6. What project management methodologies do you prefer and why?

The choice depends on project requirements, team dynamics, organizational culture, and client preferences. Agile methodologies like Scrum are preferable due to their adaptability and ability to accommodate changing requirements.

7. How was your experience in college and your key learnings in the four years of Engineering?

Engineering programs are known for their challenging coursework. Students often learn to manage heavy workloads, prioritize tasks, and develop strong problem-solving skills. Engineering projects often require collaboration with peers from diverse backgrounds. Students learn to work effectively in teams, communicate ideas clearly, and leverage each other's strengths to achieve common goals. Overall, college can be a transformative experience for engineering students, providing them with the knowledge, skills, and mindset needed to succeed in their careers.

8. What do you think, is the arrival of "Devin" like a devil for software engineers?

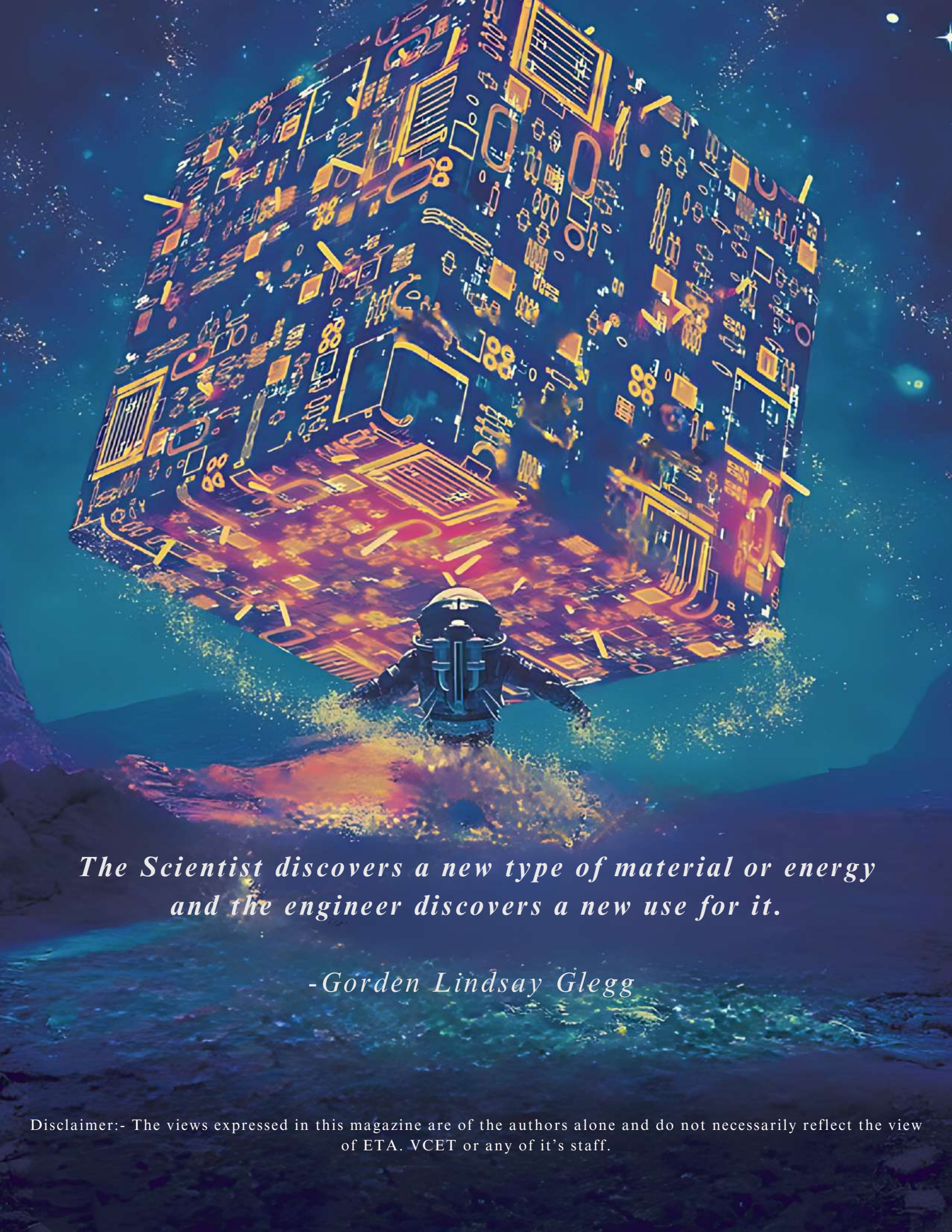
Software engineers are accustomed to adapting to new technologies, methodologies, and challenges as part of their profession. While certain developments may pose difficulties initially, they often lead to opportunities for growth and innovation in the long run.

9. How do you stay connected with our college and other alumni, and what are the benefits or opportunities that you get from doing so?

Many colleges and universities have official social media pages and groups where alumni can connect and stay updated on news, events, and opportunities. staying connected with college and alumni networks offers numerous benefits, including professional networking, mentorship, career opportunities, personal growth, and a sense of belonging to a larger community. By actively engaging with their alma mater and fellow graduates, individuals can leverage these networks to support their personal and professional goals throughout their lives.

10. If you wanted to go back to your past and wanted to correct something or wanted to give a piece of particular advice to yourself what would it be?

Take care of your physical, mental, and emotional health. Make time for activities that bring you joy, relaxation, and fulfillment. Cultivate meaningful connections with family, friends, mentors, and colleagues. Nurture these relationships with empathy, communication, and support. Building a strong support network can provide invaluable guidance and encouragement.



The Scientist discovers a new type of material or energy and the engineer discovers a new use for it.

-Gorden Lindsay Glegg