University of Mumbai

Examination 2021 under cluster 5(Lead College: APSIT)

Examinations Commencing from 01st June 2021

Program: Electronics and Telecommunication Engineering

Curriculum Scheme: Rev2016

Examination: TE Semester VI

Course Code: ECCDLO 6021 and Course Name: Digital VLSI Design

Time: 2 hour Max. Marks: 80

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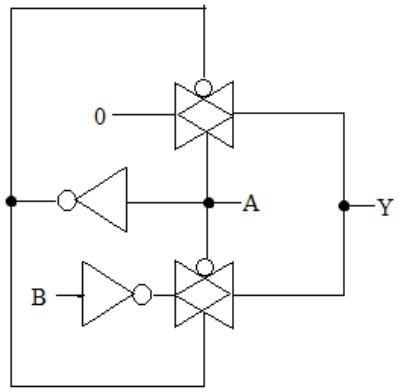
Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	Which of the following statement is not true?
Option A:	Two metal lines can cross each other at the same layer
Option B:	When a polysilicon crosses a diffusion region, it represents a MOSFET
Option C:	Stick diagrams do not represent dimensions of MOSFET
Option D:	Stick diagrams do not represent parasitic in the circuit
2.	What of the following is not a feature of Static CMOS design style?
Option A:	Low power consumption
Option B:	Smaller area requirement
Option C:	Implementation of complement expression
Option D:	Good noise margin
3.	 The above circuit is
Option A:	NOR gate
Option B:	NAND gate
Option C:	XOR gate
Option D:	AND gate
4.	Which of the following is not a dynamic design style
Option A:	Domino logic
Option B:	NORA logic
Option C:	C^2MOS logic
Option D:	Pseudo nMOS logic
5.	The loss of output voltage level due to charge sharing problem in dynamic CMOS

	design can be prevented using
Option A:	Voltage bootstrapping
Option B:	Evaluation transistor
Option C:	Weak pull-up
Option D:	Parallel output capacitor
6.	In a NOR based ROM, data bit '1' is stored using,
Option A:	Absence of a transistor
Option B:	Presence of a transistor
Option C:	Series combination of transistor
Option D:	Parallel combination of transistor
7.	SRAM stores data using,
Option A:	Charge on the capacitor
Option B:	Modulating threshold voltage of a MOSFET
Option C:	Magnetic field
Option D:	Cross coupled inverters
8.	What of the following is true about NAND flash and NOR flash,
Option A:	NOR flash has better fabrication density than NAND flash
Option B:	NOR flash have faster read operations
Option C:	In NAND flash, cells are connected in parallel
Option D:	NOR flash endure for more erase cycles than NAND flash
9.	Carry Select Adder overcomes latency by,
Option A:	Avoiding rippling of carry from LSB to MSB
Option B:	Aiding the propagation of carry bit around an adder
Option C:	Simultaneous MSB-half addition with both possible values of LSB-half carry
Option D:	Predicting the carry
10.	What is the formula for calculating carry bit c_{i+1} in the addition of a_i and b_i using Carry Look Ahead Adder?
Option A:	$a_i.b_i$
Option B:	$c_i \oplus p_i$
Option C:	$g_i + p_i c_i$
Option D:	$a_i \oplus b_i$
11.	Which of the following is the best suitable for addition of 7 multi-bit numbers
Option A:	Carry Skip Adder
Option B:	Carry Look Ahead Adder
Option C:	Ripple Carry Adder
Option D:	Carry Save Adder
12.	The output of 8X4 barrel shifter after performing 3 bit logical left shift operation on 11010111
Option A:	1101
Option B:	0101
Option C:	1011
Option D:	0111

13.	IO Circuits and clock generation and distribution do not determine,
Option A:	Feature size
Option B:	Signal Integrity
Option C:	Compatibility with other IC technology
Option D:	Inter IC communication speed
14.	Random skew, drift and jitter form the clock distribution network are proportional to
Option A:	The clock frequency
Option B:	The network delay
Option C:	The duty cycle of the clock
Option D:	Circuit architecture
15.	The essence of ESD protection is,
Option A:	To provide a controlled discharge path for high voltage to avoid damaging of gate oxide
Option B:	To create a barrier to avoid damaging of gate oxide
Option C:	To provide a controlled discharge path for high voltage to avoid damaging of diffusion region
Option D:	To create a barrier to avoid damaging of diffusion region
16.	Capacitive or inductive coupling causes interference called,
Option A:	Dispersion
Option B:	Return path effect
Option C:	Crosstalk
Option D:	Inter Symbolic Interference
17.	Programmable Array Logic (PAL) have,
Option A:	Fixed AND plane and programmable OR plane
Option B:	Fixed AND plane and fixed OR plane
Option C:	Programmable AND plane and fixed OR plane
Option D:	Programmable AND plane and programmable OR plane
18.	FPGA stands for
Option A:	Fast Programmable Gate Array
Option B:	Field Programmable Gate Array
Option C:	Fast Programmable Gate Arrangement
Option D:	Field Programmable Gate Arrangement
19.	What is the proper sequence of the steps to design a Custom Single Purpose Processor
Option A:	HLSM-Controller FSM-Datapath Design- Connect the datapath to controller
Option B:	HLSM- Connect the datapath to controller - Datapath Design-Controller FSM
Option C:	HLSM-Datapath Design-Controller FSM - Connect the datapath to controller
Option D:	HLSM-Datapath Design-Connect the datapath to controller-Controller FSM
20.	How does controller FSM differ from HLSM?
Option A:	FSM have fewer states than HLSM
Option B:	Condition for state transition in FSM is a signal status, whereas HLSM have logical condition

Option C:	FSM do not have external control inputs, HLSM have external control inputs
Option D:	In FSM state transition can happen without an event, in HLSM the transition can happen only on the occurrence of an event

Q2	
A	**Solve any Two** **05 marks each**
i.	Implement 4X4 NAND based ROM array to store '1001', '0011', '0101', '0010' in the memory
ii.	Implement 4:1 MUX using transmission gate
iii.	Write HDL code for D Flip Flop with asynchronous 'Reset' input. If the reset signal is '1', the output is '0'.
B	**Solve any One** **10 marks each**
i.	Draw JK flip flop using CMOS and explain the working.
ii.	Draw 3-T DRAM Cell and explain the following operations in brief with appropriate diagram. a) Write '1' b) Write '0' c) Read '1' d) Read ''0
Q3.	
A	**Solve any Two** **05 marks each**
i.	Explain ESD in brief Explain any one protection network with appropriate diagram.
ii.	Implement a Full Adder using PAL.
iii.	Draw a 3 bit array multiplier.
B	**Solve any One** **10 marks each**
i.	Explain the Carry Look Ahead Adders in brief. Write the expression for carry generate and propagate circuit for 4 bit adder. Implement the same using domino logic.
ii.	Design a 'Laser Based Distance Measurement System' using the RTL design process.