Curriculum Scheme: Revised 2019

Examination: Second Year Semester III

Course Code and Course Name: Digital Electronics - ISC304

Time: 2hour Max. Marks: 80

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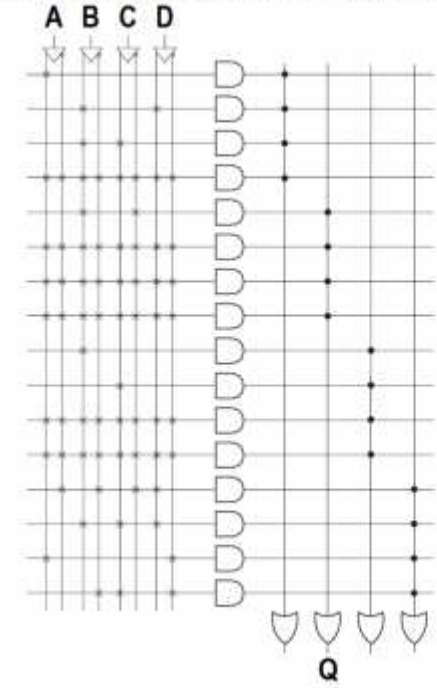
Q1.	Solve the following
1	Simplify the given Boolean expression ABC+A'B+ABC' to minimum number of literals
Option A:	B
Option B:	1
Option C:	ABC+A'B+AB
Option D:	A
2	x + yz = (x + y)(x + z) is
Option A:	De Morgan's Theorem
Option B:	The associative law
Option C:	The commutative Law
Option D:	The distributive law
3.	How many entries will be there in the truth table of a 3 input NAND gate?
Option A:	3
Option B:	6
Option C:	9
Option D:	8
4	What is the Minterm equivalent of A' + B'
Option A:	∑(0,1)
Option B:	∑(0,1,2)
Option C:	∑(1,2)
Option D:	∑(1,2,3)
5	Which of the following expression is dual of (A + B) (C + D) = AC + AD + BC + BD
Option A:	(AB + CD) = (A + C) (A + D) (B + C) (B + D)
Option B:	(AC + BD) = (A + C) (A + D) (B + C) (B + D)
Option C:	(AB + CD) = (A + B) (A + D) (B + C) (C + D)
Option D:	(AD + BC) = (A + B) (A + C) (B + C) (B + D)
6	The following Boolean function equivalent to. F(x, y, z) = Σ(0, 2, 4, 5, 6)
Option A:	xy+z'

Option B:	z’
Option C:	z’+xy’
Option D:	xy
7	The following Boolean function equivalent to. F(A, B, C, D) = π(1, 3, 5, 7, 13, 15)
Option A:	BD’+ACD’
Option B:	BD’+ACD’+ABC’D
Option C:	(B+D’)(A+C+D’)
Option D:	(A+D’)(B’+D’)
8	For a logic family, given that V_{OH} is the minimum output high level voltage V_{OL} is the maximum output low level voltage V_{IH} is the minimum acceptable input high level voltage V_{IL} is the maximum acceptable input low level voltage Then correct relation ship is
Option A:	$V_{IH} > V_{OH} > V_{IL} > V_{OL}$
Option B:	$V_{OH} > V_{IH} > V_{IL} > V_{OL}$
Option C:	$V_{OH} > V_{IH} > V_{OL} > V_{IL}$
Option D:	$V_{OH} < V_{IH} < V_{IL} < V_{OL}$
9.	A full adder can be realized using
Option A:	one half adder, two AND gates
Option B:	two half adders, one OR gate
Option C:	two half adders, one AND gate
Option D:	two half adders, two AND gates
10	Which of the following is not a property of CMOS logic gates?
Option A:	High switching speed
Option B:	Low static power consumption
Option C:	High packing density
Option D:	High noise margin
11	The number of 2:1 multiplexers required to implement 8:1 multiplexer is
Option A:	6
Option B:	7
Option C:	8
Option D:	9
12	A RAM is
Option A:	Non-volatile memory
Option B:	Volatile memory
Option C:	Static and dynamic memory
Option D:	Volatile and either static or dynamic memory
13	How many address and data lines is there in 1M×16 ROM system?
Option A:	20 and 4

Option B:	20 and 16
Option C:	10 and 4
Option D:	10 and 16
14	What function is implemented at output Q of the following PAL structure? 
Option A:	BD +BC + A
Option B:	B + C
Option C:	ABCD + A'B'C'D'
Option D:	BC'
15	A combinational logic circuit
Option A:	must contain flip-flops
Option B:	may contain flip-flops
Option C:	does not contain flip-flops
Option D:	contains latches
16	The output Qn of a J-K flip-flop is 0.Its output does not change when a clock pulse is applied. The inputs Jn and Kn are respectively.
Option A:	X and 0
Option B:	0 and 0
Option C:	0 and X
Option D:	1 and 1
17	A binary ripple counter uses flip□flops that trigger on the positive□edge of the clock. What will be the count if the normal outputs of the flip□flops are connected to the clock input of the next stage.
Option A:	Down counter
Option B:	BCD counter
Option C:	Up counter
Option D:	Gray code sequence generator

18	The minimum number of flipflops required to design a mod10 ripple counter is
Option A:	10
Option B:	7
Option C:	4
Option D:	5
19	While converting a JK flip-flop to D flip-flop, instead of connecting an inverter between its J and K inputs, a buffer has been connected. The resulting circuit will act as
Option A:	JK flip flop only
Option B:	SR flip flop
Option C:	D flip flop
Option D:	T flip flop
20	$(FFF.DA)_{16}$ is equivalent to (?) in binary
Option A:	110111011101.10011000
Option B:	111011101110.10101100
Option C:	111111111111.11011010
Option D:	101110111011.11001010

Q2 **(20 Marks)**	**Solve any Four out of Six** **5 marks each**
A	Implement EX-OR by using NOR as universal
B	Design and implement full Subtractor.
C	Define specification of logic family
D	Design and implement MOD 4 counter
E	Write short note on PAL.
F	Differentiate between combinational and sequential logic

Q3. **(20 Marks)**	**Solve any Two Questions out of Three** **10 marks each**
A	Convert following equation into standard SOP form 1)AB+ABC+AC 2)AC+AD+ACD+ABC
B	Design and implement BCD to excess-3 code converter.

C	Design 4 bit Asynchronous up counter using JK flip flop