Vidyavardhini's College of Engineering & Technology, Vasai(w)

Department of Electronics & Telecommunication Engineering

Subject: Microprocessor and Peripherals
SEM V (ECC501) (REV-2016)

Q No	Questions
	Module I: Introduction to Microcomputer
1	_____ converts the programs written in assembly language into machine instructions. a) Machine compiler b) Interpreter c) Assembler d) Converter Explanation: An assembler is a software used to convert the programs into machine instructions.
2	The coded object modules of the program to be assembled are present in a) .ASM file b) .OBJ file c) .EXE file d) .OBJECT file solution : .OBJ file is created with same name as source file and extension .OBJ. It contains the coded object modules of the program to be assembled.
3	The extension that is essential for every assembly level program is a) .ASP b) .ALP c) .ASM d) .PGM solution : every assembly level program should have extension .asm
4	**Compiler translates the source code to** a. **Executable code** b. **Assembly code** c. **Binary code** d. Non executable code
5	Which bus carry addresses a. Address bus b. Data bus c. Control bus d. System bus. Solution : address bus is used to carry address of memory or port
6	20 bit address can generate an addresss upto

	a. 1KB b. 1 GB c. 1MB d. 1 TB Solution: $2^{20} = 2^{10} \times 2^{10}$ = 1KB X 1KB=1MB
7.	CPU can read, write data by using a. Address bus b. Data bus c. Control bus d. System bus. Solution : a. CPU can read, write data by using Data bus
8.	Which bus can generate Read, Write signals a. Address bus b. Data bus c. Control bus d. System bus. Solution : Control bus can generate Read, Write signals
9.	When memory read or IO read are achieved data is to the processor a. Input b. Output c. Input / output d. Can't say Solution : memory read or IO read are with respect to microprocess read ie input data
10	When memory Write or IO Write are achieved data is to the processor a. Input b. Output c. Input / output d. Can't say Solution: memory Write or IO Write are with respect to microprocess read ie output data
	Module II Architecture of 8086 microprocessor
11	**Which of the following is/are 16-bit micro processor?** a) 8008 b) 8080 c) 8085

	d) 8086 solution 8086 is 16 bit microprocessor
12	**The register of 8086 are_____ bits in size.** a) 8 b) 12 c) 16 d) 20 **solution :The register of 8086 are 16 nit size as it is 16 bit processor**
13	**Which register is used as a default counter in case of string and loop instructions.** a) AX b) BX c) CX d) DX **Solution: CX register is used as a default counter in case of string and loop instructions.**
14	**The number of address and data lines of 8086_____.** a) 8 and 8 b) 16 and 16 c) 20 and 16 d) 16 and 20 solution : size of address bus 20 bit and data bus is 16 bit
15.	**_____ contains the actual assembly language instructions to be executed by the microprocessor.** a) Data segment b) Code segment c) Stack segment

	d) Extra segment
16	**Instruction Pointer (IP) contains offset address of which segment ?** a) Data segment b) Code segment c) Stack segment d) Extra segment
17	**Which of the following is not a machine control flag?** a) Direction flag b) Interrupt flag c) Overflow flag d) Trap flag solution: Overflow flag is conditional flag
18	BHE of 8086 microprocessor signal is used to interface the_____ a) I/O b) DMA c) Even bank memory d) Odd bank memory solution : **If BHE'=0, then it indicates the transfer of data over the higher order data bus i.e. D8-D15. The higher order bus is interfaced to odd address bank memory when BHE' is enabled.**
19	Ready pin of a microprocessor is used_____ a) To indicate that processor is ready to receive inputs outputs b) To indicate that processor is ready to receive inputs output c) To introduce wait states d) To provide direct memory access. Solution : **Explanation: This input is controlled to insert wait states into the timing of the microprocessor.**

20	The _____ input is examined by a ‘wait’ instruction. a) K b) TEST c) LOCK d) KIT **Explanation: TEST’ input is examined by WAIT instruction. When TEST’ goes low, execution will continue, else, the processor remains in an idle state.**
	Module III : Instruction Set and programming of 8086
21	Which segment register is being used in the given instruction? MOV CX , SS: [BX] a) Extra Segment Register (ES) b) Code Segment Register (CS) c) Stack Segment Register (SS) d) None of the Above **Answer: c. Stack Segment Register (SS)** **Explanation:** Here, the concept of Segment Override Prefix is being used. Although the default segment for the offset BX is DS, as the SS is mentioned in the instruction, it is overriding the default segment. Hence, the Stack Segment (SS) register is being used here.
22	Which segment register is being used in the given instruction? MOV CX , [IP] a) Extra Segment Register (ES) b) Code Segment Register (CS) c) Stack Segment Register (SS) d) None of the Above **Answer: b. Code Segment Register (CS)** **Explanation:** Here, the default segment for the offset IP is CS. Hence, the Code Segment (CS) register is being used here.
23	Which of the following is not a data copy/transfer instruction? a) MOV

	b) PUSH c) DAS d) POP Answer: c Explanation: DAS (Decimal Adjust after Subtraction) is an arithmetic instruction.
24	Which of the following instruction is not valid? a) MOV AX, BX b) MOV DS, 5000H c) MOV AX, 5000H d) PUSH AX Answer: b Explanation: Both the source and destination operands cannot be memory locations except for string instructions.
25	Which of the following assembler directives are used to define a Procedure in the 8086 microprocessor? 1. PROCEDURE and ENDP 2. STARTP and ENDP 3. PROC and ENDPROC 4. PROC and ENDP **Answer: d.** **Explanation:** The assembler directive that are used for defining a procedure in the 8086 microprocessor are: PROC and ENDP.
26	In a program, a Macro is being called 'n' times. Then how many times is the machine code generated for the same? 1. 1 time 2. 'n' times 3. 'n-1' times 4. n+1 **Answer: b. 'n' times** **Explanation:**

	The machine code (containing the instructions within the Macros) is generated every time the macro is called. So, if a Macro is being called 'n' times, then the number of times the machine code is generated is also 'n'?
27	DEBUG is able to troubleshoot only a) EXE files b) OBJ files c) EXE file and .OBJ file e) EXE flie and .LST file Answer: Option A
28	The purpose of the ORIGIN directive is _____ a) To indicate the starting position in memory, where the program block is to be stored b) To indicate the starting of the computation code c) To indicate the purpose of the code d) To list the locations of all the registers used Answer: Option A
29	Which of the following features is not offered by Macros? a) Code reusability b) Less memory space c) Fast execution d) Slow execution **Answer: b. Less Memory Space** **Explanation:** Every time a Macro is invoked, the entire set of instructions is loaded into the main memory due to which the execution of macros takes large memory space.
30	LES copies word from memory to register and ---------- **a)** DS **b)** SS **c)** CS **d)** ES **Explanation: d)**

	Module IV: Peripherals Interfacing with 8086 and applications
31	In 8086 microprocessor one of the following statements is not true. a) Coprocessor is interfaced in MAX mode b) Coprocessor is interfaced in MIN mode c) I/O can be interfaced in MAX / MIN mode d) Supports pipelining Ans-Coprocessor is interfaced in MIN mode
32	. In 8086 microprocessor the following has the highest priority among all type interrupts. a) NMI b) DIV 0 c) TYPE 255 d) OVER FLOW Ans-a) NMI
33	**In which mode do all the Ports of the 8255 PPI work as Input-Output units for data transfer?** 1. BSR mode 2. Mode 0 of I/O mode 3. Mode 1 of I/O mode 4. Mode 2 of I/O mode **Answer: b. Mode 0 of I/O mode**
34	**How many data lines in total are there in the 8255 PPI IC?** **1. 8 data lines** **2. 32 data lines** **3. 24 data lines** **4. None of the above**

	Answer: c. 24 data lines
35	**If the programmable counter timer 8254 is set in mode 1 and is to be used to count six events, the output will remain at logic 0 for _____ number of counts** **A) 5** **B) 6** **C) 0** **D) 8** **Ans. OUT continues for the total length of the count. Hence answer is (B).**
36	**Which PORT C pins are used for port B in 8255 mode 1:** **a. PC0-PC2** **b. PC3-PC7** **c. PC6-PC7** **d. PC3-PC5** **Ans. a**
37	**What is size of I/O ports in 8255** **A.8 Bits** **B. 16 Bits** **C. 4 Bits** **D. 2 Bits** **Ans. a**
38	**Which chip used for interfacing peripherals with 8086 processor:** **a. 8251** **b. 8255** **c. 8254**

	d. 8259 **Ans. b**
39	**___ bit in ICW1 indicates whether the 8259A is cascade mode or not?** **a) LTIM=0** **b) LTIM=1** **c) SNGL=0** **d) SNGL=1** **Ans-SNGL=0**
40	**The pin that clears the control word register of 8255 when enabled is** **a) CLEAR** **b) SET** **c) RESET** **d) CLK** **Answer: c** **Explanation: If reset pin is enabled then the control word register is cleared.**
	Module V ADC, DAC, Interfacing with 8086 and its application
41	**which multiplexer by ADC 0808/0809:** **a. 2:4** **b. 3:8** **c. 4:16** **d. 5:32** **Ans-b**
42	**Which of the following statements are true about DAC0808**

	a) parallel digital data to analog data conversion **b) it has current as an output** **c) both of the mentioned** **d) Can't say** **Ans-a**
43	**The conversion delay in successive approximation of an ADC 0808/0809 is** **a) 100 milliseconds** **b) 100 microseconds** **c) 50 milliseconds** **d) 50 milliseconds** **Answer: b** **Explanation: The conversion delay is 100microseconds which is low as compared to other converters**
44	**In ADC 0809 acting as a CMOS device, how many analog inputs & channel multiplexers are present?** **A. 2** **B. 4** **C. 8** **D. 16** **Ans-C.8**
45	8 input DAC has **a)** 8 discrete levels **b)** 16 discrete levels **c)** 128 discrete levels **d)** 256 discrete levels Solution : 2^n discrete levels 2^8=256
	Module VI: 8087 math coprocessor and memory interfacing
1	To operate 8087 in maximum mode, the pin MN/MX is a) connected to Vcc or power supply b) connected to ground

	c) left unconnected d) none of the mentioned Answer: b Explanation: The 8087 can operate in a maximum mode, only when the MN/MX (active low) pin of the CPU is grounded. In maximum mode, all the control signals are derived using a sequence chip known as a bus controller.
2	Why 8087 is referred to as Coprocessor? i) Because 8087 is used in parallel with main processor in a system, rather than serving as a main processor itself. ii) Because 8087 is used in serial with main processor in a system, rather than serving as a main processor itself. iii) Because main Microprocessor handles the general program execution and the 8087 handles specialized math computations. a) i & iii b) ii & iii c) iii only. d) i only.
3	The coprocessors operate in _____ with a processor on the same buses and with the same instruction _____. a) Parallel, byte stream. b) Series, byte stream. c) Series, bite stream d) Parallel, bite stream.
4	If the microprocessor has 10 address lines, then the number of memory locations it is able to address is a) 512 b) 1024 c) 2048 d) none
5	Number of chips required to design 32KB using 16KB is a) 1 b) 2 c) 3 d) 4