Examination: SE Semester III

Course Code: CSC304 and Course Name: DL&COA

Time: 2-hour Max. Marks: 80

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<table>
<tr><td>Q1.</td><td>Choose the correct option for following questions. All the Questions are compulsory and carry equal marks</td></tr>
<tr><td></td><td></td></tr>
<tr><td>1.</td><td>_____ number of clock cycles are required to process 200 tasks in a six-segment pipeline.</td></tr>
<tr><td>Option A:</td><td>204</td></tr>
<tr><td>Option B:</td><td>205</td></tr>
<tr><td>Option C:</td><td>206</td></tr>
<tr><td>Option D:</td><td>207</td></tr>
<tr><td></td><td></td></tr>
<tr><td>2.</td><td>Which of the examples below expresses the commutative law of multiplication?</td></tr>
<tr><td>Option A:</td><td>A + B = B + A</td></tr>
<tr><td>Option B:</td><td>A • B = B + A</td></tr>
<tr><td>Option C:</td><td>A • B = B • A</td></tr>
<tr><td>Option D:</td><td>A • (B • C) = (A • B) • C</td></tr>
<tr><td></td><td></td></tr>
<tr><td>3.</td><td>Von Neumann machine is an example of _____.</td></tr>
<tr><td>Option A:</td><td>multiple instruction multiple data</td></tr>
<tr><td>Option B:</td><td>multiple instruction single data</td></tr>
<tr><td>Option C:</td><td>single instruction multiple data</td></tr>
<tr><td>Option D:</td><td>single instruction single data</td></tr>
<tr><td></td><td></td></tr>
<tr><td>4.</td><td>Consider a 2-level memory hierarchy of the form (m1, m2), where m1 is directly connected to the CPU.
<table>
<tr><td>Level(I)</td><td>Capacity (Si)</td><td>Cost (Ci)</td></tr>
<tr><td>M1(Cache)</td><td>1024</td><td>0.1000</td></tr>
<tr><td>M2(Main)</td><td>2^{16}</td><td>0.0100</td></tr>
</table>
Determine the average cost per bit.</td></tr>
<tr><td>Option A:</td><td>0.01138</td></tr>
<tr><td>Option B:</td><td>0.11138</td></tr>
<tr><td>Option C:</td><td>0.21138</td></tr>
<tr><td>Option D:</td><td>0.31138</td></tr>
<tr><td></td><td></td></tr>
<tr><td>5.</td><td>MUL R1, R2 is _____ instruction.</td></tr>
<tr><td>Option A:</td><td>one byte</td></tr>
<tr><td>Option B:</td><td>two bytes</td></tr>
<tr><td>Option C:</td><td>three bytes</td></tr>
<tr><td>Option D:</td><td>four bytes</td></tr>
<tr><td></td><td></td></tr>
<tr><td>6.</td><td>After interface of 4KB memory with CPU by using 1KB chip of RAM, CPU gives _____ address lines.</td></tr>
<tr><td>Option A:</td><td>10</td></tr>
</table>

<table>
<tr><td>Option B:</td><td>11</td></tr>
<tr><td>Option C:</td><td>12</td></tr>
<tr><td>Option D:</td><td>13</td></tr>
<tr><td></td><td></td></tr>
<tr><td>7.</td><td>Consider a 4-stage pipeline processor. The number of cycles needed by the four instructions I1, I2, I3 and I4 in stages S1, S2, S3 and S4 is shown below-
<table>
<tr><td></td><td>S1</td><td>S2</td><td>S3</td><td>S4</td></tr>
<tr><td>I1</td><td>2</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>I2</td><td>1</td><td>3</td><td>2</td><td>2</td></tr>
<tr><td>I3</td><td>2</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>I4</td><td>1</td><td>2</td><td>2</td><td>2</td></tr>
</table>
What is the number of cycles needed to execute (i=1 to 4) {I1; I2; I3; I4;} loop?</td></tr>
<tr><td>Option A:</td><td>16</td></tr>
<tr><td>Option B:</td><td>23</td></tr>
<tr><td>Option C:</td><td>28</td></tr>
<tr><td>Option D:</td><td>30</td></tr>
<tr><td></td><td></td></tr>
<tr><td>8.</td><td>When the processor receives the request from a device, it responds by sending _____.</td></tr>
<tr><td>Option A:</td><td>Acknowledge signal</td></tr>
<tr><td>Option B:</td><td>BUS grant signal</td></tr>
<tr><td>Option C:</td><td>Response signal</td></tr>
<tr><td>Option D:</td><td>None of the mentioned</td></tr>
<tr><td></td><td></td></tr>
<tr><td>9.</td><td>If size of main memory is 4MB, size of cache memory is 64KB, block size is 32*8 then to interface cache memory with main memory number of blocks in main memory are ____.</td></tr>
<tr><td>Option A:</td><td>107213</td></tr>
<tr><td>Option B:</td><td>131072</td></tr>
<tr><td>Option C:</td><td>141072</td></tr>
<tr><td>Option D:</td><td>151072</td></tr>
<tr><td></td><td></td></tr>
<tr><td>10.</td><td>The following switching functions are to be implemented using a decoder:
f1 = ∑m(1, 2, 4, 8, 10, 14) f2 = ∑m(2, 5, 9, 11) f3 = ∑m(2, 4, 5, 6, 7)
The minimum configuration of decoder will be _____.</td></tr>
<tr><td>Option A:</td><td>2 to 4 line</td></tr>
<tr><td>Option B:</td><td>3 to 8 line</td></tr>
<tr><td>Option C:</td><td>4 to 16 line</td></tr>
<tr><td>Option D:</td><td>5 to 32 line</td></tr>
<tr><td></td><td></td></tr>
<tr><td>11.</td><td>How many NAND circuits are contained in a 7400 NAND IC?</td></tr>
<tr><td>Option A:</td><td>8</td></tr>
<tr><td>Option B:</td><td>4</td></tr>
<tr><td>Option C:</td><td>2</td></tr>
<tr><td>Option D:</td><td>1</td></tr>
<tr><td></td><td></td></tr>
</table>

12.	Memory address of direct cache mapping with main memory 64K words, cache memory 2K words, block size 16 words have ___, ____, and _____ of TAG, LINE and WORD fields, respectively.
Option A:	7, 4, and 5 bits
Option B:	4, 5, and 7 bits
Option C:	5, 4, and 7 bits
Option D:	5, 7, and 4 bits
13.	How many two input AND gates and two input OR gates are required to realize Y = BD + CE + AB?
Option A:	3, 2
Option B:	2, 3
Option C:	3, 3
Option D:	2, 2
14.	When the processor receives the request from a device, it responds by sending _____.
Option A:	Acknowledge signal
Option B:	BUS grant signal
Option C:	Response signal
Option D:	None of the mentioned
15.	Exclusive-OR (XOR) logic gates can be constructed from what other logic gates?
Option A:	OR gates only
Option B:	AND gates and NOT gates
Option C:	AND gates, OR gates, and NOT gates
Option D:	OR gates and NOT gates
16.	The disadvantage of the hardwired approach is _____.
Option A:	It is very flexible
Option B:	It cannot be used for complex instructions
Option C:	It is costly
Option D:	less flexible & cannot be used for complex instructions
17.	The canonical sum of product form of the function y (A, B) = A + B is _____.
Option A:	AB + BB + A'A
Option B:	AB + AB' + A'B
Option C:	BA + BA' + A'B'
Option D:	AB' + A'B + A'B'
18.	If the control memory has 128 bits, then the size of address field in microinstruction format is _____ bits.
Option A:	8
Option B:	7
Option C:	6
Option D:	5
19.	MAR ← (PC) MDR ← Memory

	PC ← (PC) + 1 IR ← (MDR) This is the sequence of micro-operations in _____.
Option A:	fetch cycle
Option B:	execute cycle
Option C:	interrupt cycle
Option D:	indirect cycle
20.	Complement of the expression A'B + CD' is _____.
Option A:	(A' + B) (C' + D)
Option B:	(A + B') (C' + D)
Option C:	(A' + B) (C' + D)
Option D:	(A + B') (C + D')

Q2	**Solve any Two Questions out of Three** **10 mark each**
A	Explain different technique for design of control unit of computer.
B	Design 4-bit BCD adder using IC 7483.
C	What is micro program? Write microprogram for following operations I. ADD R1, M, Register R1 and Memory location M are added and result store at Register R1. II. MUL R1, R2 Register R1 and Register R2 are multiplied and result store at Register R1.

Q3	
A	**Solve any Two** **5 mark each**
i.	Simplify A+A'B+A'B'C+A'B'C'D using Boolean laws.
ii.	Explain memory interleaving Techniques.
iii.	Explain IEEE 754 floating point representation formats and represent (34.25)10 to single precision format.
B	**Solve any One** **10 mark each**
i.	Realize the operation using only NAND gates. F (A, B, C, D) = π M (0, 2, 3, 6, 7, 8, 9, 12, 13)
ii.	Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 10 ns. Calculate- 1. Pipeline cycle time 2. Non-pipeline execution time 3. Speed up ratio 4. Pipeline time for 1000 tasks