Program: Information Technology

Curriculum Scheme: Revised **2012**

Examination: Third Year Semester **V**

Course Code: **TEITC503** and Course Name: **MICROCONTROLLER AND EMBEDDED SYSTEMS**

Time: 1hour Max. Marks: 50

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Note to the students:- All the Questions are compulsory and carry equal marks .

Q1.	Which is the first company who defined RISC architecture?
Option A:	Intel
Option B:	IBM
Option C:	Motorola
Option D:	MIPS
Q2.	To initialize any port as an output port what value is to be given to it?
Option A:	0xFF
Option B:	0x00
Option C:	0x01
Option D:	A port is by default an output port
Q3.	LCALL instruction takes
Option A:	2 bytes
Option B:	4 bytes
Option C:	3 bytes
Option D:	1 bytes
Q4.	Each instruction in ARM machines is encoded into _____ Word.
Option A:	2 bytes
Option B:	3 bytes
Option C:	4 bytes
Option D:	8 bytes
Q5.	Which of the following uses its own address space?
Option A:	thread
Option B:	process
Option C:	task
Option D:	kernel
Q6.	The time taken to respond to an interrupt is known as
Option A:	interrupt delay
Option B:	interrupt time

Option C:	interrupt latency
Option D:	interrupt function
Q7.	The instructions which are used to load or store multiple operands are called as _____
Option A:	Banked instructions
Option B:	Lump transfer instructions
Option C:	Block transfer instructions
Option D:	DMA instructions
Q8.	JZ, JNZ, DJNZ, JC, JNC instructions monitor the bits of which register?
Option A:	DPTR
Option B:	B
Option C:	A
Option D:	PSW
Q9.	What is the advantage of register indirect addressing mode?
Option A:	it makes use of registers R0 and R1
Option B:	it uses the data dynamically
Option C:	it makes use of operator @
Option D:	it is easy
Q10.	Which of the following statements are true for von Neumann architecture?
Option A:	shared bus between the program memory and data memory
Option B:	separate bus between the program memory and data memory
Option C:	external bus for program memory and data memory
Option D:	external bus for data memory only
Q11.	What is 80/20 rule?
Option A:	80% instruction is generated and 20% instruction is executed
Option B:	80% instruction is executed and 20% instruction is generated
Option C:	80%instruction is executed and 20% instruction is not executed
Option D:	80% instruction is generated and 20% instructions are not generated
Q12.	On power up, the 8051 uses which RAM locations for register R0- R7
Option A:	00 - 2F
Option B:	00 - 07
Option C:	00 - 7F
Option D:	00 - 0F
Q13.	ANL instruction is used _____
Option A:	to AND the contents of the two registers
Option B:	to mask the status of the bits
Option C:	All of the mentioned
Option D:	None of the mentioned

Q14.	The banked registers are used for _____
Option A:	Switching between supervisor and interrupt mode
Option B:	Extended storing
Option C:	Same as other general purpose registers
Option D:	None of the mentioned
Q15.	Which of the following defines the set of instructions loaded into the memory?
Option A:	process
Option B:	task
Option C:	thread
Option D:	system hardware
Q16.	Which of the following is inherited from the parent task?
Option A:	task
Option B:	process
Option C:	thread
Option D:	kernel
Q17.	The effective address of the instruction written in Post-indexed mode, MOVE[Rn]+Rm is _____
Option A:	EA = [Rn]
Option B:	EA = [Rn + Rm]
Option C:	EA = [Rn] + Rm
Option D:	EA = [Rm] + Rn
Q18.	When the call instruction is executed the topmost element of stack comes out to be
Option A:	the address where stack pointer starts
Option B:	the address next to the call instruction
Option C:	address of the call instruction
Option D:	next address of the stack pointer
Q19.	Which addressing mode is used in pushing or popping any element on or from the stack?
Option A:	immediate
Option B:	direct
Option C:	indirect
Option D:	register
Q20.	Which of the following has a Harvard architecture?
Option A:	EDSAC
Option B:	SSEM
Option C:	PIC
Option D:	CSIRAC

Q21.	How is memory accessed in RISC architecture?
Option A:	load and store instruction
Option B:	opcode instruction
Option C:	memory instruction
Option D:	bus instruction
Q22.	Are PUSH and POP instructions are a type of CALL instructions?
Option A:	yes
Option B:	no
Option C:	None of the mentioned
Option D:	can't be determined
Q23.	Which of the following registers are not bit addressable?
Option A:	SCON
Option B:	PCON
Option C:	A
Option D:	PSW
Q24.	Which of the following does not uses a shared memory?
Option A:	process
Option B:	thread
Option C:	task
Option D:	kernel
Q25.	The addressing mode where the EA of the operand is the contents of Rn is _____
Option A:	Pre-indexed mode
Option B:	Pre-indexed with write back mode
Option C:	Post-indexed mode
Option D:	None of the mentioned