

Program: BE Information Technology

Curriculum Scheme: Revised 2016

Examination: Second Year Semester III

Course Code: ITC302

Course Name: Logic Design

Time: 1 hour

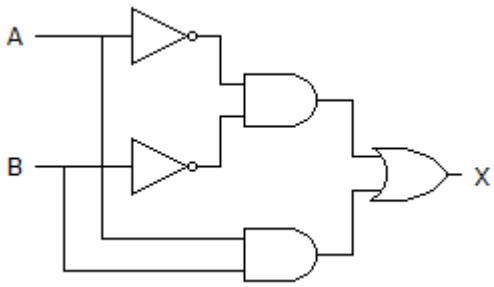
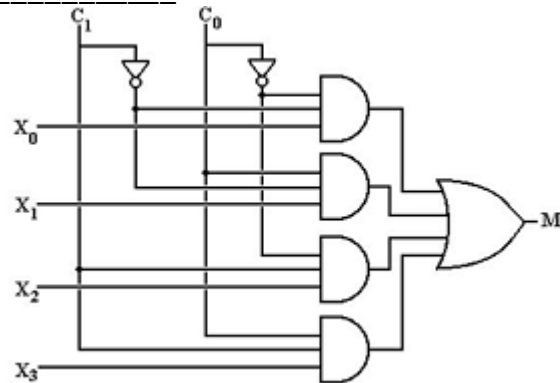
Max. Marks: 50

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Note to the students:- All the Questions are compulsory and carry equal marks .

Q1.	A BJT has $\alpha=0.99$. Find the value of β .
Option A:	100
Option B:	99
Option C:	200
Option D:	199
Q2.	The stability factor of voltage divider bias circuit depends on
Option A:	Beta value
Option B:	Beta and Base resistor value
Option C:	Beta, Base resistor and Collector resistor value
Option D:	Beta, Base resistor and Emitter resistor value
Q3.	Find the binary representation of $(13.625)_{10}$
Option A:	1101.101
Option B:	101.1101
Option C:	110.1101
Option D:	1011.101
Q4.	Convert $(23.46)_8$ to hexadecimal representation
Option A:	17.89
Option B:	31.48
Option C:	13.98
Option D:	32.64
Q5.	2's complement of 98 is
Option A:	01100010
Option B:	10011101
Option C:	10011110
Option D:	01100011
Q6.	BCD code of 48 is
Option A:	00110000
Option B:	01001000
Option C:	11010000
Option D:	10000100

Q7.	Find Gray code of 101101101
Option A:	111011011
Option B:	011011011
Option C:	101101111
Option D:	100101001
Q8.	A fixed bias circuit has following parameters. Calculate its stability factor. $V_{CC} = 15V, R_C = 1k\Omega, R_B = 20k\Omega, \alpha = 0.995$
Option A:	100
Option B:	99
Option C:	200
Option D:	199
Q9.	Which of the following is an universal gate
Option A:	AND
Option B:	OR
Option C:	EX-OR
Option D:	NAND
Q10.	In SOP (Sum of Products) form Level 1 is of _____ gates and Level 2 is of _____ gates.
Option A:	AND and OR
Option B:	AND and NAND
Option C:	OR and AND
Option D:	NOR and NAND
Q11.	Simplify $Y = \sum_m(0, 3, 4, 7)$ using K-map
Option A:	$\bar{B}\bar{C} + BC$
Option B:	$A\bar{C} + BC$
Option C:	$\bar{A}\bar{C} + \bar{B}C$
Option D:	$A\bar{B} + B\bar{C}$
Q12.	Simplify $(A + \bar{B} + AB)(A + \bar{B})(\bar{A}B)$
Option A:	$A + \bar{B}$
Option B:	A
Option C:	0
Option D:	$\bar{A}\bar{B}$
Q13.	Which of the following is a 4-bit binary adder?
Option A:	IC7404
Option B:	IC7483
Option C:	IC7485
Option D:	IC7408

Q14.	What is the logical expression of the following circuit 
Option A:	$\overline{A}\overline{B} + AB$
Option B:	$\overline{A}B + A\overline{B}$
Option C:	$A\overline{B} + AB$
Option D:	$\overline{A}\overline{B} + A\overline{B}$
Q15.	How many 3-line-to-8-line decoders are required for a 1-of-32 decoder?
Option A:	1
Option B:	2
Option C:	4
Option D:	8
Q16.	Which of the following combinations cannot be combined into K-map groups?
Option A:	Corners in the same row
Option B:	Corners in the same column
Option C:	Overlapping combinations
Option D:	Diagonal corners
Q17.	In the given 4-to-1 multiplexer, if $c_1 = 0$ and $c_0 = 1$ then the output M is 
Option A:	x_0
Option B:	x_1
Option C:	x_2
Option D:	x_3
Q18.	On a positive edge-triggered S-R flip-flop, the outputs reflect the input condition when _____
Option A:	The clock pulse is LOW

Option B:	The clock pulse is HIGH
Option C:	The clock pulse transitions from LOW to HIGH
Option D:	The clock pulse transitions from HIGH to LOW
Q19.	How many states does a decimal counter has?
Option A:	10
Option B:	11
Option C:	8
Option D:	16
Q20.	How many flip-flops are required to construct a decade counter?
Option A:	10
Option B:	8
Option C:	5
Option D:	4
Q21.	How can parallel data be taken out of a shift register simultaneously?
Option A:	Use the Q output of the first FF
Option B:	Use the Q output of the last FF
Option C:	Tie all of the Q outputs together
Option D:	Use the Q output of each FF
Q22.	Which is not characteristic of a shift register?
Option A:	Serial in/parallel in
Option B:	Serial in/parallel out
Option C:	Parallel in/serial out
Option D:	Parallel in/parallel out
Q23.	In VHDL, which of the following is the basic building block of a design?
Option A:	Architecture
Option B:	Entity
Option C:	Process
Option D:	Package
Q24.	Which of the following describes the structure of VHDL code correctly?
Option A:	Entity Declaration; Configuration; Library Declaration; Architecture Declaration
Option B:	Library Declaration; Configuration; Entity Declaration; Architecture Declaration
Option C:	Library Declaration; Entity Declaration; Architecture Declaration; Configurations
Option D:	Configuration; Library Declaration; Entity Declaration; Architecture Declaration
Q25.	Which of the following can be the name of an entity in VHDL?
Option A:	AND
Option B:	NAND
Option C:	NAND_gate
Option D:	NAND gate