1) The I/O interface required to connect the I/O device to the bus consists of _____
a) Address decoder and registers
b) Control circuits
c) Address decoder, registers and Control circuits
d) Only Control circuits

2) The control unit controls other units by generating _____
a) Control signals
b) Timing signals
c) Transfer signals
d) Command Signals

3) During the execution of a program which gets initialized first?
a) MDR
b) IR
c) PC
d) MAR

4) Which category includes traditional uniprocessors?
a) SISD
b) SIMD
c) MISD
d) MIMD

5) The registers, ALU and the interconnection between them are collectively called as _____
a) process route
b) information trail
c) information path
d) data path

6) CPU consists of the following Functional Units:
a) CU
b) ALU
c) Both
d) None

7) If there are 8 data lines then the size of Data Bus is
a)8
b) 16
c) 24

d) None

8) The decimal value 0.5 in IEEE single precision floating point representation has

a) A fraction bit of 000…000 and exponent value of 0
b) B fraction bits of 000…000 and exponent value of −1
c) C fraction bits of 100…000 and exponent value of 0
d) D no exact representation

9) The range of integers that can be represented by an n bit 2's complement number system is
a) - 2n - 1 to (2n - 1 - 1)
B) - (2n - 1 - 1) to (2n - 1 - 1)
C) - 2n - 1 to 2n - 1
D) - (2n - 1 + 1) to (2n - 1 + 1)

10) What is the default value of accumulator in booth's multiplication of two 4-bit binary numbers?
a) 0
b) 1
c) 0000
d) 00000

11) Which of the following is often called the double precision format?
a) 64-bit
b) 8-bit
c) 32-bit
d) 128-bit

12) In Booth's algorithm, for Multiplier=10000 and Multiplicand =1100101. How much number of cycles are required to get the correct multiplication result?
a. 4
b. 5
c. 3
d. 6

13) What is the range of bias exponent in double precision representation of floating point number?
a. 0 to 255
b. 0 to 1023
c. 0 to 256
d. 0 to 127

14) The instruction ADD 3030 is of

a) A 3-address instruction format
b) A 2-address instruction format
c) A 1-address instruction format
d) A 0-address instruction format

15) Which category of microprocessor instructions detect the status conditions in registers and accordingly exhibit the variations in program sequence on the basis of detected results?
a. Transfer Instructions
b. Operation Instructions
c. Control Instructions
d. All of the above

16) The pseudo instruction used to load an address into the register is _____
a) LOAD
b) ADR
c) ASSIGN
d) PSLOAD

17) The disadvantage of CISC design processors is
a) low burden on compiler developers
b) wide availability of existing software
c) complex in nature
d) none

18) Which of the following is an application of RISC architecture by adding more instructions?
a) multimedia applications
b) telecommunication encoding
c) image conversion
d) all of the mentioned

19) There are _____ general purpose registers in 8085 processor
A. 5
B. 6
C. 7
D. 8

20) MVI K, 20F is an example of?
A. Immediate addressing mode

B. Register addressing mode
C. Direct addressing mode
D. Indirect addressing mode

21) Which of the following is the fastest means of memory access for CPU?
a) Registers
b) Cache
c) Main memory
d) Virtual Memory

22) _____ storage is a system where a robotic arm will connect or disconnect off-line mass storage media according to the computer operating system demands.
a) Secondary
b) Virtual
c) Tertiary
d) Magnetic

23) The effectiveness of the cache memory is based on the property of _____
a) Locality of reference
b) Memory localisation
c) Memory size
d) None of the mentioned

24) The write-through procedure is used _____
a) To write onto the memory directly
b) To write and read from memory simultaneously
c) To write directly on the memory and the cache simultaneously
d) None of the mentioned

25) The DMA differs from the interrupt mode by _____
a) The involvement of the processor for the operation
b) The method of accessing the I/O devices
c) The amount of data transfer possible
d) None of the mentioned

26) When the R/W bit of the status register of the DMA controller is set to 1.
a) Read operation is performed
b) Write operation is performed
c) Read & Write operation is performed
d) None of the mentioned

27) To overcome the conflict over the possession of the BUS we use _____
a) Optimizers
b) BUS arbitrators
c) Multiple BUS structure
d) None of the mentioned

28) Joysticks typically have a button on _____that is used to select the option pointed by the cursor.
A.Bottom
B.Left
C.Right
D.Top

29) Which device of computer operation dispenses with the use of the keyboard?
A.Joystick
B.Light pen
C.Mouse
D.Touch

30) A light sensitive device that converts drawing, printed text or other images into digital form is A.Keyboard
B.Plotter
C.Scanner
D.OMR

31) Each stage in pipelining should be completed within _____ cycle.
a) 1
b) 2
c) 3
d) 4

32) The computer architecture aimed at reducing the time of execution of instructions is _____
a) CISC
b) RISC
c) ISA
d) ANNA

33) When the processor executes multiple instructions at a time it is said to use _____

a) single issue
b) Multiplicity
c) Visualization
d) Multiple issues

34) In super-scalar processors, _____ mode of execution is used.
a) In-order
b) Post order
c) Out of order
d) None of the mentioned