**Computer Engg/Sem-III/CBCGS/DLDA_SQP**

1) The representation of octal number (532.2)8 in decimal is _____

a) (346.25)10
b) (532.864)10
c) (340.67)10
d) (531.668)10

2) Convert the binary number (01011.1011)2 into decimal:

a) (11.6875)10
b) (11.5874)10
c) (10.9876)10
d) (10.7893)10

3) On subtracting (010110)2 from (1011001)2 using 2's complement, we get _____

a) 0111001
b) 1100101
c) 0110110
d) 1000011

4) On addition of -33 and -40 using 2's complement, we get _____

a) 1001110
b) -110101
c) 0110001
d) -1001001

5) Gray code equivalent of the decimal number (243.17)10 is _____.

a) (10001010.00111)
b) (10101010.10101)
c) (10010010.01010)
d) (10000101.11000)

6) The excess-3 code for 597 is given by _____

a) 100011001010
b) 100010100111
c) 010110010111
d) 010110101101

7) De-Morgan's theorem states that _____

a) (AB)' = A' + B'
b) (A + B)' = A' * B
c) A' + B' = A'B'
d) (AB)' = A' + B

8) The Boolean function A + BC is a reduced form of _____

a) AB + BC
b) (A + B)(A + C)
c) A'B + AB'C
d) (A + C)B

9) The expression Y=AB+BC+AC shows the _____ operation.

a) EX-OR
b) SOP
c) POS
d) NOR

10) The canonical sum of product form of the function y(A,B) = A + B is _____

a) AB + BB + A'A
b) AB + AB' + A'B
c) BA + BA' + A'B'
d) AB' + A'B + A'B'

11) Product-of-Sums expressions can be implemented using _____

a) 2-level OR-AND logic circuits
b) 2-level NOR logic circuits
c) 2-level XOR logic circuits
d) Both 2-level OR-AND and NOR logic circuits

12) How many full adders are required to construct an m-bit parallel adder?

a) m/2
b) m
c) m-1
d) m+1

13) How many AND gates are required to realize Y = CD + EF + G?

a) 4
b) 5
c) 3
d) 2

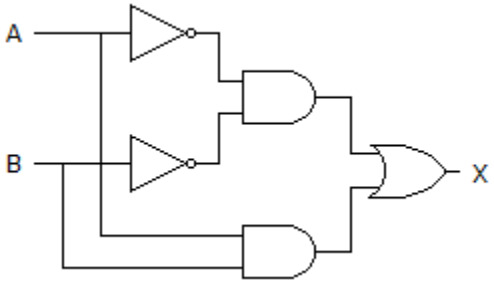
14) Which of following are known as universal gates?

a) NAND & NOR
b) AND & OR
c) XOR & OR
d) EX-NOR & XOR

15) How many NAND circuits are contained in a 7400 NAND IC?

a) 1
b) 2
c) 4
d) 8

16) What type of logic circuit is represented by the figure shown below?




a) XOR
b) XNOR
c) AND
d) XAND

17) A combinational circuit is one in which the output depends on the _____

a) Input combination at the time
b) Input combination and the previous output
c) Input combination at that time and the previous input combination
d) Present output and the previous output

18) A D flip-flop can be constructed from an _____ flip-flop.

a) S-R
b) J-K
c) T
d) S-K

19) In a J-K flip-flop, if J=K the resulting flip-flop is referred to as _____

a) D flip-flop
b) S-R flip-flop
c) T flip-flop
d) S-K flip-flop

20) One of the major drawbacks to the use of asynchronous counters is that _____

a) Low-frequency applications are limited because of internal propagation delays
b) High-frequency applications are limited because of internal propagation delays

c) Asynchronous counters do not have major drawbacks and are suitable for use in high- and low-frequency counting applications
d) Asynchronous counters do not have propagation delays, which limits their use in high-frequency applications

21) How many flip-flops are required to construct a decade counter?
a) 4
b) 8
c) 5
d) 10

22) A ripple counter's speed is limited by the propagation delay of _____
a) Each flip-flop
b) All flip-flops and gates
c) The flip-flops only with gates
d) Only circuit gates

23) How many clock pulses will be required to completely load serially a 5-bit shift register?
a) 2
b) 3
c) 4
d) 5

In a VHDL program, the architecture can have more than one entity.
a) True
b) False

24) In composite data type of VHDL, the record type comprises the elements of _____data types.
a) Same
b) Different
c) Both a and b
d) None of the above

25) Which of the following logic families has the shortest propagation delay?
a) A.CMOS
b) B.BiCMOS
c) C.ECL
d) D.74SXX

26) What should be done to unused inputs on TTL gates?
a) They should be left disconnected so as not to produce a load on any of the other circuits and to minimize power loading on the voltage source.

b) All unused gates should be connected together and tied to V through a 1 k resistor.
c) All unused inputs should be connected to an unused output; this will ensure compatible loading on both the unused inputs and unused outputs.
d) Unused AND and NAND inputs should be tied to VCC through a 1 k resistor; unused OR and NOR inputs should be grounded.

27) Why must CMOS devices be handled with care?
a) so, they don't get dirty
b) because they break easily
c) because they can be damaged by static electricity discharge

28) Which type of device FPGA are?
a) SLD
b) SROM
c) EPROM
d) PLD

29) How many logic gates can be implemented in the circuit by complex programmable logic devices (CPLDs)?
a) 10
b) 100
c) 1000
d) 10000