Design of 8 Bit Hybrid Carry Save Adder

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***Abstract*— Adder is a digital circuit that performs the basic function of addition. It is an essential part of every digital circuit. It is used in computers to compute addresses and in ALUs. The most time critical application of adder is in Digital Signal Processing, where it is used to compute Fast Fourier Transforms, multiplier outputs, etc. This often involves three or more inputs to the adder. One of the adders capable of computing 3 or more inputs is the Carry Save Adder (CSA). The main flaw of conventional Carry Save Adder is that it uses Ripple Carry Adder (RCA) in its last stage to compute the output, thus making it slow. In this paper a new, hybrid design of Carry Save Adder is proposed, which employs Carry Look Ahead Adder (CLA) in the last stage thus making carry generation much faster and improving overall delay of the Carry Save Adder.**

***Keywords*— Adder, Carry Save Adder (CSA), Ripple Carry Adder (RCA), Carry Look Ahead Adder (CLA), Hybrid Adder.**

I. Introduction

In today's VLSI circuit design industry, high speed and low power consumption is of key importance. One of the important digital VLSI circuits is adder. An adder is a basic calculator used to find the sum of 2 binary numbers. Adders are used in processors, ALUs to calculate memory addresses and other similar operations. There are two types of basic adders:

A. Half Adder

Half Adder is an electronic circuit that performs addition of two numbers. In half adder, addition of two single bit binary digits takes place and sum and carry outputs are generated. Half adder is a combinational logic circuit which is implemented by using one XOR gate and one AND gate as shown in Fig. 1.1. The sum is obtained from XOR gate output and carry is obtained from AND gate output.

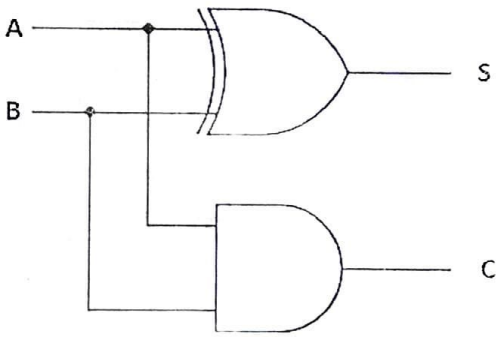

Fig. 1.1. Gate Level Design of Half Adder

B. Full Adder

Full Adder is a circuit that performs addition of two binary numbers and a carry input. If a carry is generated from the previous stage the carry input is logic 1 and if carry is not generated from the previous stage then carry is logic 0. Full adder, as shown in Fig. 1.2, is designed by using two XOR gates, two AND gates and one OR gate. Full adder circuit has three inputs and generates two outputs.

ISBN: 978-93-5659-047-2

PRABODHAN SHIKSHAN PRASARAK SANSTHA'S (Regd. No. E-697 Ratnagiri)

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4th National Conference on

"Changing Technology and Rural Development"

CTRD 2022

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